

ATTACHMENT 2

AEC - Q200-002 REV-B

HUMAN BODY MODEL ELECTROSTATIC DISCHARGE TEST

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Component Technical Committee

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METHOD - 002

PASSIVE COMPONENT HUMAN BODY MODEL (HBM) ELECTROSTATIC DISCHARGE (ESD) TEST

1. SCOPE

1.1 Description:

The purpose of this specification is to establish a reliable and repeatable procedure for determining *PASSIVE COMPONENT* HBM ESD sensitivity.

1.2 Reference Documents:

IEC 61000-4-2
ISO 10605

1.3 Terms and Definitions:

The terms used in this specification are defined as follows.

1.3.1 Component Failure:

A condition in which a component does not meet all the requirements of the acceptance criteria, as specified in section 5 following the ESD test.

1.3.2 Device Under Test (DUT):

An electronic component being evaluated for its sensitivity to ESD.

1.3.3 Electrostatic Discharge (ESD):

The transfer of electrostatic charge between bodies at different electrostatic potentials.

1.3.4 Electrostatic Discharge Sensitivity:

An ESD voltage level which causes component failure.

1.3.5 ESD Simulator:

An instrument that simulates the *PASSIVE COMPONENT* human body model ESD pulse as defined in this specification.

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1.3.6 Ground Plane:

A common electrical reference point for the DUT, ESD simulator, and auxiliary equipment.

1.3.7 Human Body Model (HBM):

A capacitance and resistance model that characterizes a person as a source of electrostatic charging for automotive conditions, as shown in Figure 1, and the resulting ESD pulse meeting the waveform criteria specified in this test method.

1.3.8 Maximum Withstanding Voltage:

The maximum ESD voltage at which, and below, the component is determined to pass the failure criteria requirements specified in Section 4.

1.3.9 PUT:

PUT is the pin and/or terminal under test.

2. EQUIPMENT:

2.1 Test Apparatus:

The apparatus for this test consists of an ESD pulse simulator with an equivalent **PASSIVE COMPONENT** HBM ESD circuit as shown in Figure 1. The simulator must be capable of supplying pulses which meet the waveform requirements of Table 1 and Figure 3 using the coaxial target specified in Section 2.2.1.

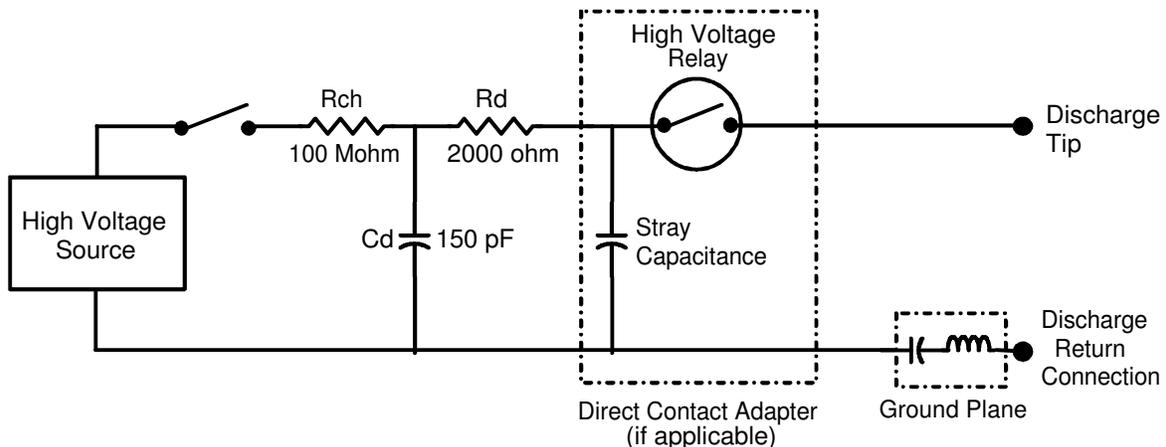


Figure 1: Equivalent *PASSIVE COMPONENT* HBM ESD simulator circuit

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2.2 Measurement Equipment:

Equipment used to verify conformance of the simulator discharge waveform to the requirements as specified in Table 1 and Figure 3 shall be either an analog oscilloscope with a minimum bandwidth of 1.0GHz or a digital oscilloscope with a minimum sampling rate of 2 gigasamples per second and a minimum bandwidth of 1.0GHz. Each instrument shall have 50Ω input impedance. A faster oscilloscope (larger bandwidth and/or higher sampling rate) may be required to fully characterize the ESD waveform.

2.2.1 Coaxial Target:

The coaxial target shall be a current-sensing transducer as specified by IEC 61000-4-2, or equivalent. The target is used to verify the ESD simulator waveform as defined in Sections 2.3, 2.3.1, and 2.3.2.

2.2.2 Ground Plane:

The ground plane is a common electrical reference point with dimensional requirements of a 1mm minimum thickness and a 1m² minimum area. The ground plane is connected to earth ground by a ground strap as short and as wide as possible; length ≤ 1m, width ≥ 5mm, and inductance ≤ 2μH.

2.2.3 Probe:

The probe used to verify the ESD simulator charging voltage, as defined in Sections 2.3.2 and 2.4, shall be an electrometer probe with an input impedance ≥ 100 Gigohm.

2.2.4 20 dB Wideband Attenuator:

A 20 dB wideband attenuator may be required depending on the vertical sensitivity of the oscilloscope. The attenuator shall be a 50Ω, 20dB wideband attenuator with a bandwidth of 20GHz and 2kW peak pulse power. When using the attenuator, it shall be attached to the output of the coaxial target during the ESD simulator qualification and waveform verification as defined in Sections 2.3 and 2.4.

2.3 ESD Simulator Qualification:

ESD simulator calibration and qualification must be performed during initial acceptance testing and whenever the simulator is serviced. A period of six (6) months is the maximum permissible time between full qualification tests. The ESD simulator must meet the waveform parameter requirements for all voltage levels as defined in Table 1, Section 2.3.1, and Section 2.3.2. If at any time the waveforms do not meet the requirements of Table 1 and Figure 3, the testing shall be halted until waveforms are in compliance.

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2.3.1 Simulator Qualification Setup:

- a. The simulator qualification setup shall be configured according to the equivalent schematic shown in Figure 2. Note that a 20dB wideband attenuator may be required as shown in Figure 2 depending on the vertical sensitivity of the oscilloscope.
- b. The coaxial target shall be located on and bonded to the center of the ground plane. The target output shall be connected to the oscilloscope through a 50Ω double-shielded, high frequency, semi-rigid cable with length $\leq 1\text{m}$. The cable shall not be looped and shall be insulated from the ground plane.
- c. The horizontal time base and vertical amplifier level of the oscilloscope shall be configured in order to view the risetime of the ESD waveform. The horizontal sweep shall be set to single event trigger.
- d. The ESD simulator high voltage ground shall be directly connected to the ground plane by a grounding strap with length $\leq 1\text{m}$ and an inductance $\leq 2\mu\text{H}$. The ESD simulator shall be set up and operated according to its instruction manual.

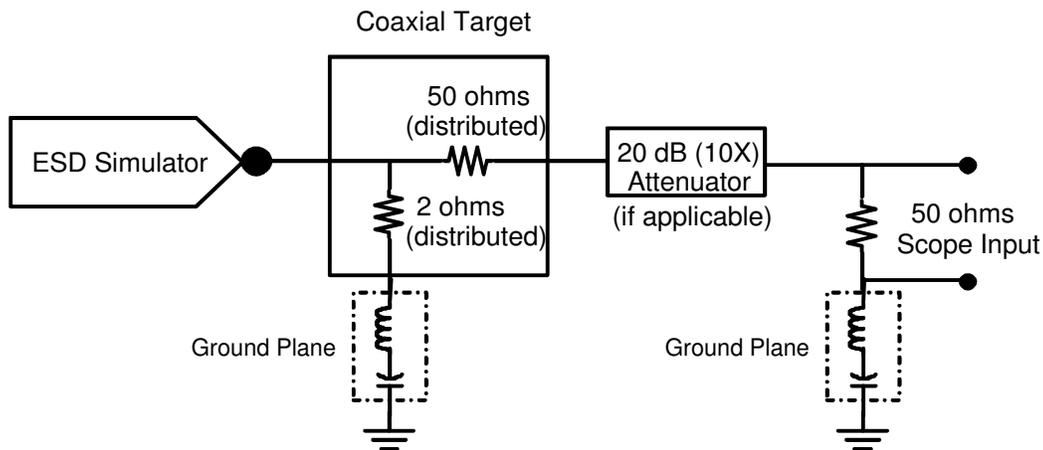


Figure 2: Equivalent schematic for Simulator Qualification

2.3.2 Simulator Qualification Procedure:

- a. To calibrate the display voltage of the ESD simulator, adjust the simulator voltage to the desired level and polarity. With the electrometer in direct contact with the discharge tip (see Figure 1), verify the voltage setting at levels of $\pm 500\text{V}$, $\pm 1\text{kV}$, $\pm 2\text{kV}$, $\pm 4\text{kV}$, $\pm 8\text{kV}$, $\pm 12\text{kV}$, $\pm 16\text{kV}$, and $\pm 25\text{kV}$. The electrometer reading shall be within $\pm 10\%$ for voltages from 200V to $\leq 25\text{kV}$.
- b. For Direct Contact Discharge Qualification, discharge to the coaxial target at each voltage level and polarity shown in Table 1. Record the risetime and first peak current values and verify the parameters meet the requirements of Table 1. Figure 3 illustrates a typical discharge waveform to a coaxial target. The simulator must meet the requirements of Table 1 and Figure 3 for five (5) consecutive waveforms at all voltage levels.

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- c. For Air Discharge qualification, the ESD simulator shall be placed a distance of $\geq 15\text{mm}$ from the coaxial target sphere. The ESD simulator, with the air discharge probe attached, shall be held perpendicular ($\pm 15^\circ$) to the target. From this position, the simulator air discharge probe shall be slowly ($\leq 5\text{mm/second}$) moved towards the target until a single discharge occurs. Only single event discharge waveforms shall be acceptable. Test voltages for the air discharge are $\pm 12\text{kV}$, $\pm 16\text{kV}$, and $\pm 25\text{kV}$. Figure 3 illustrates a typical discharge waveform to a coaxial target. The slow approach method specified above minimizes multiple discharges, discharges at lower voltage levels, and ringing in the measurement equipment.

2.4 ESD Simulator Charge Verification:

The performance of the simulator can be dramatically degraded by parasitics in the discharge path. Therefore, to ensure proper simulation and repeatable ESD results, ESD simulator charge verification shall be performed before each daily use. With the electrometer in direct contact with the discharge tip (see Figure 1), verify the voltage setting at levels of $\pm 500\text{V}$, $\pm 1\text{kV}$, $\pm 2\text{kV}$, $\pm 4\text{kV}$, $\pm 8\text{kV}$, $\pm 12\text{kV}$, $\pm 16\text{kV}$, and $\pm 25\text{kV}$. The electrometer reading shall be within $\pm 10\%$ for voltages from 200V to $\leq 25\text{kV}$. If at any time the simulator charge does not meet the requirements of Table 1, the testing shall be halted until the simulator is in compliance and all ESD testing performed since the last passing charge verification shall be considered invalid.

Table 1: Direct Contact and Air Discharge ESD Waveform Parameter Requirements

ESD Discharge Method	Indicated Voltage (kV)	First Peak Current, I_p (A)	Rise Time, t_r (ns)
Direct Contact Discharge	0.5 ± 0.05	$1.87 +0.60/-0$	0.7 to 1.0
	1.0 ± 0.1	$3.75 +1.12/-0$	0.7 to 1.0
	2.0 ± 0.5	$7.50 +2.25/-0$	0.7 to 1.0
	4.0 ± 0.5	$15.0 +4.50/-0$	0.7 to 1.0
	8.0 ± 0.8	$30.0 +9.0/-0$	0.7 to 1.0
Air Discharge	25.0 ± 2.5	Not Specified	Not Specified

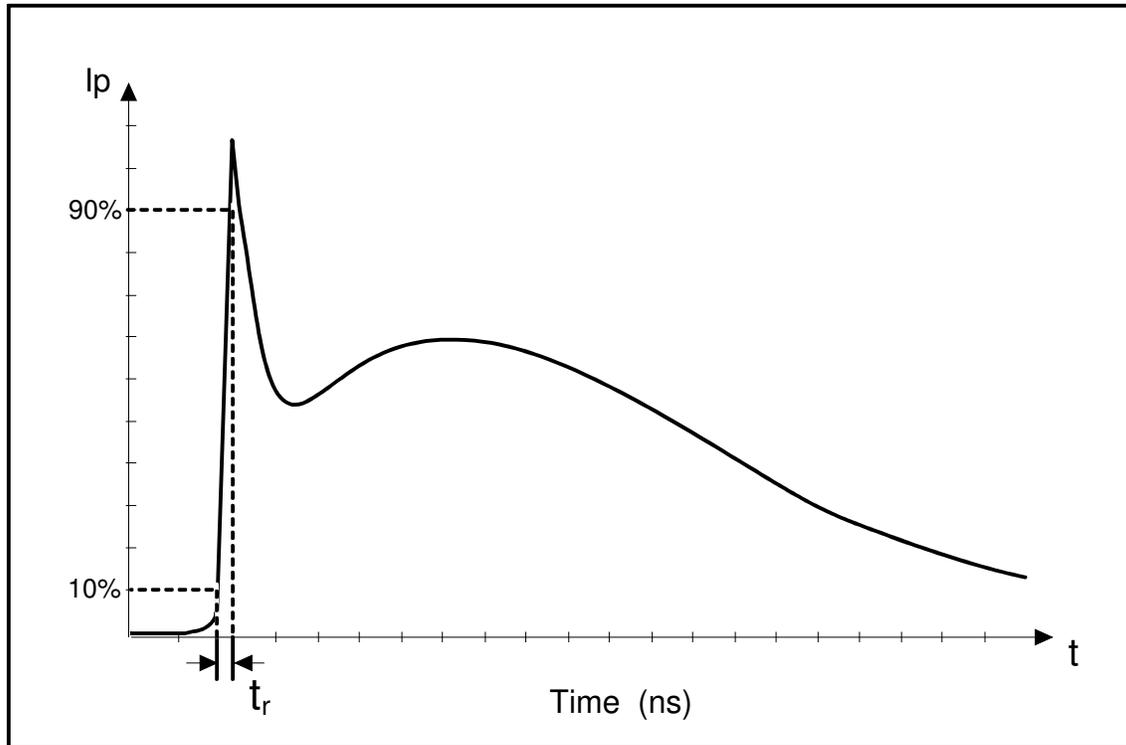


Figure 3: Typical Direct Contact and Air Discharge *PASSIVE COMPONENT* HBM ESD Discharge Waveform to a Coaxial Target

3. TEST PROCEDURE:

3.1 Sample Size:

Each sample group shall be composed of 15 components, as specified in Table 1 of AEC-Q200. Each sample group shall be stressed at one (1) voltage level using all pin and/or terminal combinations specified in Section 3.2. The use of a new sample group for each stress voltage level is recommended. It is permitted to use the same sample group for the next stress level if all components in the sample group meet the acceptance criteria requirements specified in Section 5 after exposure to a specified voltage level.

3.2 Pin and/or Terminal Combinations:

Each pair of pins and/or terminals and all combinations of pin and/or terminal pairs for each component shall be subjected to one (1) pulse at each stress voltage polarity following the ESD levels stated in Figure 4. Any pin and/or terminal not under test shall be in an electrically open (floating) state. A sufficient number of ESD levels must be tested to either: a) demonstrate the component can pass a 25kV Air Discharge exposure, or b) determine the pass/fail transition region between two (2) consecutive ESD test levels. If an expected failure level cannot be estimated, the test flow diagram of Figure 4 may be used to minimize the amount of testing required.

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3.3 Test Environment:

Each component shall be subjected to ESD pulses at $22^{\circ}\text{C} \pm 5^{\circ}\text{C}$. For all Air Discharge testing, the relative humidity shall be 30% to 60%.

3.4 Measurements:

Prior to ESD testing, complete parametric testing (initial electrical verification) shall be performed on all sample groups and all components in each sample group per applicable user device specification at room temperature followed by hot temperature, unless specified otherwise in the user device specification. If using an allowable parametric shift as failure criteria, a data log of each component shall be made listing the applicable parameter measurement values. The data log will be compared to the parameters measured during final electrical test verification testing to determine the failure criteria of Section 4.

3.5 Test Setup:

- a. Ensure that the daily ESD simulator charge verification procedure (Section 2.4) has been performed before applying discharges to the DUT.
- b. The ESD simulator high voltage ground shall be directly connected to the ground plane by a grounding strap with a length $\leq 1\text{ m}$ and an inductance $\leq 2\mu\text{H}$.
- c. All DUT's are considered sensitive to ESD until proven otherwise and shall be handled accordingly (reference internal procedures for proper handling of ESD sensitive components).
- d. The DUT must pass complete parametric testing (initial electrical verification) as defined in Section 3.4 prior to any application of ESD stress voltage levels.

3.6 Detailed Procedure:

3.6.1 Direct Contact Discharge:

- a. The ESD simulator shall be placed in direct contact with each PUT specified in Section 3.2.
- b. Each PUT within a sample group shall be tested at a stress voltage level specified in the test flow diagram of Figure 4 using the Direct Contact discharge probe. Two (2) discharges shall be applied to each PUT within a sample group and at each stress voltage level, one (1) with a positive polarity and one (1) with a negative polarity.
- c. After each discharge to the PUT, residual charge remaining on the DUT shall be dissipated by briefly connecting a one (1) megohm resistor between the PUT discharge location and/or ground point of the DUT and the ground of the test setup.
- d. Repeat the procedure for all components within the sample group.

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- e. Using the next sample group, select another direct contact stress voltage level and repeat the above procedure until all sample groups have been tested at a specified voltage level. It is permitted to use the same sample group for the next stress voltage level if all components in the sample group meet the acceptance criteria requirements specified in Section 5 after exposure to a specified voltage level.
- f. Submit the components for complete parametric testing (final electrical verification) per the user device specification at room temperature followed by hot temperature, unless specified otherwise in the user device specification, and determine whether the components meet the acceptance criteria requirements specified in Section 5. It is permitted to perform the parametric testing (final electrical verification) per user device specification after all sample groups have been tested.

3.6.2 Air Discharge:

- a. Using a new sample group, each PUT specified in Section 3.2 shall be tested at an air discharge stress voltage level specified in the test flow diagram of Figure 4 using the Air Discharge probe. It is permitted to use the same sample group for the next stress voltage level if all components in the sample group meet the acceptance criteria requirements specified in Section 5 after exposure to a specified voltage level.
- b. The ESD simulator shall be placed $\geq 15\text{mm}$ away from the PUT. The simulator, with the Air Discharge probe, shall be held perpendicular to the PUT discharge location. The probe shall be slowly moved towards the PUT (e.g., $\leq 5\text{mm/second}$) until a single discharge is obtained.
- c. If no discharge occurs, continue moving the probe towards the DUT until the simulator discharge probe contacts the PUT discharge location. If the simulator makes contact with the PUT discharge location and discharge occurs, discontinue testing at the stress voltage level and location. A test board with closely spaced lead wires or metal runners may prevent discharging to an intended PUT and result in an arcing phenomenon. When this situation occurs, multiple test boards with a reduced number of lead wires or metal runners shall be used.
- d. Two (2) discharges shall be applied to each PUT within a sample group at the air discharge stress voltage level, one (1) with a positive polarity and one (1) with a negative polarity.
- e. After each discharge to the PUT, residual charge remaining on the DUT shall be dissipated by briefly connecting a one (1) megohm resistor between the PUT discharge location and/or ground point of the DUT and the ground of the test setup.
- f. Repeat the procedure for all components within the sample group.
- g. Using the next sample group, select another air discharge stress voltage level and repeat the above procedure until all sample groups have been tested at a specific voltage level. It is permitted to use the same sample group for the next stress voltage level if all components in the sample group meet the acceptance criteria requirements specified in Section 5 after exposure to a specified voltage level.

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- h. Submit the components for complete parametric testing (final electrical verification) per the user device specification at room temperature followed by hot temperature, unless specified otherwise in the user device specification, and determine whether the components meet the acceptance criteria requirements specified in Section 5. It is permitted to perform the parametric testing (final electrical verification) per user device specification after all sample groups have been tested.

4. FAILURE CRITERIA

A component will be defined as a failure if, after exposure to ESD pulses, the component fails any of the following criteria:

1. The component exceeds the allowable shift value. Specific parameters and allowable shift values shall be defined in the applicable user device specification. During initial parametric testing, a data log shall be made for each component listing the applicable parameter measurement values. The data log will be compared to the parameters measured during final parametric testing to determine the shift value. Components exceeding the allowable shift value will be defined as a failure.
2. The component no longer meets the user device specification requirements. Complete parametric testing (initial and final electrical verification) shall be performed per applicable user device specification.

5. ACCEPTANCE CRITERIA:

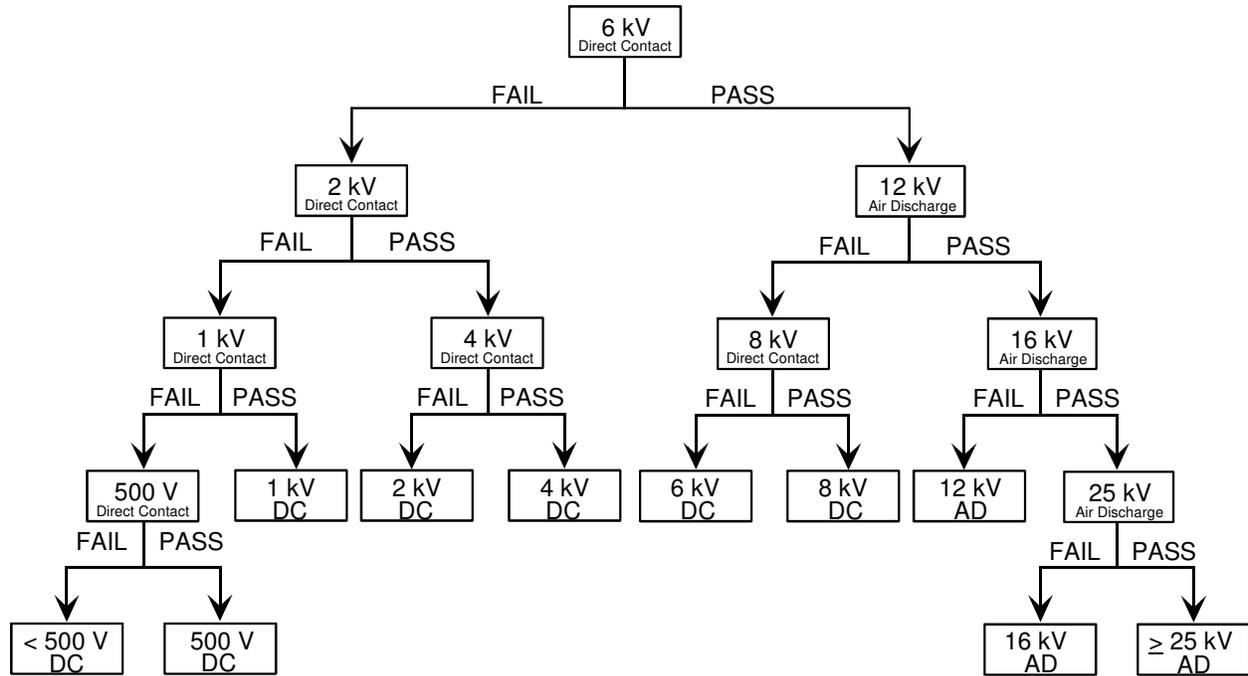
A component passes a voltage level if all components stressed at that voltage level pass. All the samples used must meet the measurement requirements specified in Section 3 and the failure criteria requirements specified in Section 4. Using the classification levels specified in Table 2, classify the components according to the highest ESD voltage level survived during ESD testing. The ESD withstanding voltage shall be defined for each component by the supplier.

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Table 2: PASSIVE COMPONENT HBM ESD Classification Levels
(DC = Direct Contact Discharge, AD = Air Discharge)

Component Classification	Maximum Withstand Voltage
1A	< 500 V (DC)
1B	500 V (DC) to < 1000 V (DC)
1C	1000 V (DC) to < 2000 V (DC)
2	2000 V (DC) to < 4000 V (DC)
3	4000 V (DC) to < 6000 V (DC)
4	6000 V (DC) to < 8000 V (DC)
5A	8000 V (DC) to < 12,000 V (AD)
5B	12,000 V (AD) to < 16,000 V (AD)
5C	16,000 V (AD) to < 25,000 V (AD)
6	≥ 25,000 V (AD)

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Note 1: Classify the components according to the highest ESD voltage level survived during ESD testing.

Figure 4: PASSIVE COMPONENT HBM ESD Test Flow Diagram
(DC = Direct Contact Discharge, AD = Air Discharge)

Revision History

<u>Rev #</u>	<u>Date of change</u>	<u>Brief summary listing affected sections:</u>
-	April 30, 1996	Initial Release.
A	March 15, 2000	Removed CDF designation throughout document. Removed Chrysler, Delco, and Ford logo from each page header. Added Component Technical Committee to each page header.
B	June 1, 2010	Notice Statement (Page 2) Added. Format Updated.