

ATTACHMENT 4

AEC - Q100-004 REV-D

IC LATCH-UP TEST

Automotive Electronics Council

Component Technical Committee

Acknowledgment

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Council would especially like to recognize the following significant contributors to the development and release of this document:

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Change Notification

The following summary details the changes incorporated into AEC-Q100-004 Rev-D:

- Referenced the latest version of the JEDEC IC Latch-up Test specification JESD78.
- Section 2, Terms and Definitions: Added definition for Maximum Stress Voltage (MSV), E-Test (Voltage Trigger Latch-up), VDD Tolerant I/O, and VSS Tolerant I/O.
- Section 4.1, General Latch-up Test Procedure, and Table 2A, Etest Addendum to JESD78 Specification Table 2, Test Matrix: Clarified use of a voltage trigger (E-test) latch-up test.
- Section 4.2.5, Record Keeping: Added guidance regarding data to be recorded and reported for latch-up testing.
- Section 5, Failure Criteria: Added detailed failure criteria that no longer exists in JEDEC78.
- Appendix A, Examples for Footnotes 2 & 4 (Table 2A): Added guidance regarding different device pins/functions and resulting MSV, Vclamp High, and Vclamp Low calculations.

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METHOD - 004

IC LATCH-UP TEST

All Latch-up testing performed on Integrated Circuit devices to be AEC Q100 qualified shall be per the latest version of the JEDEC EIA/JESD78 specification with the following clarifications and requirements (section numbers listed correspond to the JEDEC specification). Text enhancements and differences made since the last revision of this document are shown as underlined areas.

1.1 Class II Classification

All AEC Q100-004 qualification testing shall be performed with the device under test at the maximum ambient operating temperature (JEDEC - Class II).

2 Terms and Definitions

MSV (Maximum Stress Voltage): The maximum stress voltage is the maximum voltage allowed to be placed on any given pin during latch-up immunity testing without causing catastrophic damage, due to electrical over-stress (EOS) not related to latch-up, to the device. MSV is greater than the maximum operating voltage.

Note: MSV is NOT the same as the absolute maximum voltage rating from the device data sheet. MSV applies to latch-up testing only, protecting the DUT from physical damage due to stress mechanisms not directly related to latch-up. An example of an unrelated stress is one exceeding the destructive breakdown voltage of a pin resulting in EOS damage. MSV may be different for each pin and each polarity during testing, depending on process technology and circuit topology. Further, the MSV value depends on the pulse width used during latch-up testing. Shorter pulse widths may allow a higher value for MSV. Therefore, the MSV value chosen should take into account the pulse width as well as process technology and circuit topology.

E-Test (Voltage Trigger Latch-up): It is a latch-up test in which positive and negative voltage trigger pulses are applied to a pin under test. The actual test procedure shall be performed per the I-test procedure, substituting a voltage trigger for the current trigger.

VDD Tolerant I/O: Some applications require that the I/O-pin voltage be independent of the supply voltage level (higher or lower). In both cases a diode between the supply pin and I/O pin is not present, thus the I/O pin voltage will not be clamped internally. The $V_{ABS\ MAX}$ of these specific pins will be different from the other pins and could also be limited by the process. Testing above $V_{ABS\ MAX}$ would require setting the MSV according to the process limit. (MSV set by process)

VSS Tolerant I/O: Some applications require I/O pins to have a minimum voltage level less than VSS where a diode between I/O and VSS is not present. These pins must be tested to $1.5 \times V_{ABS\ MIN}$. MSV needs to be set according to the process limit. (MSV set by process)

4.1 General Latch-up Test Procedure

Products can sometimes be very sensitive to I-test pulses to the point of EOS-like failure. The E-test method provides an alternative way to evaluate the input or output of a device without causing an EOS-like event. The use of a voltage trigger (E-test) latch-up test is considered acceptable. Specific E-test parameters are indicated in Table 2A.

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Table 2A: E-test Addendum to JEDEC Specification Table 1, Test Matrix [7]

TEST TYPE	TRIGGER POLARITY	CONDITION OF UNTESTED INPUT PINS	TEST TEMPERATURE ($\pm 2^{\circ}\text{C}$)	V_{supply} CONDITION	TRIGGER TEST CONDITIONS	FAILURE CRITERIA
E-TEST	POSITIVE see FIGURE 5	Max. Logic High [1]	<u>Temperature Class II</u> Maximum ambient operating temperature	Maximum operating voltage for each V_{SUPPLY} pin group per device specification	+1.5 times max. Logic High [2,3]	$(I_{\text{NOM}} + 10\text{mA})$ or $(1.4 (I_{\text{NOM}}))$, whichever is greater [6]
		Min. Logic Low [1]				
	NEGATIVE see FIGURE 6	Max. Logic High [1]			-0.5 times max. Logic High [4,5]	
		Min. Logic Low [1]				

Notes:

- [1] Max. logic high and min. logic low shall be per the device specification. When logic levels are used with respect to a non-digital device, it means the maximum high or minimum low voltage that can be supplied to the pin per the device specification.
- [2] The trigger voltage for positive E-test is given by $V_{\text{TRIGGER}} = V_{\text{MAX}} + 0.5(V_{\text{MAX}} - V_{\text{MIN}})$ with an upper limit of $1.5(V_{\text{MAX}})$ where V_{MAX} (logic high) and V_{MIN} (logic low) are defined in JESD78 Section 2. If the Maximum Stress Voltage (MSV) for the pin (see Section 2 herein) is less than $V_{\text{MAX}} + 0.5(V_{\text{MAX}} - V_{\text{MIN}})$ or $1.5(V_{\text{MAX}})$ then the trigger voltage is given by $V_{\text{TRIGGER}} = \text{MSV}$.
- [3] Current clamped at $(I_{\text{NOM}} + 100 \text{ mA})$ or $1.5(I_{\text{NOM}})$, whichever is greater.
- [4] The trigger voltage for negative E-test is given by $V_{\text{TRIGGER}} = V_{\text{MIN}} - 0.5(V_{\text{MAX}} - V_{\text{MIN}})$ with a lower limit of $-0.5(V_{\text{MAX}})$ where V_{MAX} (logic high) and V_{MIN} (logic low) are defined in JESD78 Section 2. If the Maximum Stress Voltage (MSV) for the pin (see Section 2 herein) is less negative than $V_{\text{MIN}} - 0.5(V_{\text{MAX}} - V_{\text{MIN}})$ or $-0.5(V_{\text{MAX}})$ then the trigger voltage is given by $V_{\text{TRIGGER}} = \text{MSV}$. For VSS tolerant pins the voltage clamp must be set to $-1.5(V_{\text{MIN}})$.
- [5] Current clamped at -100 mA or $-0.5(I_{\text{NOM}})$, whichever is greater in magnitude.
- [6] If the trigger test condition reaches the voltage or current clamp limit and latch-up has not occurred, the pin passes the latch-up test. See Section 5 of the JEDEC specification for complete failure definition.
- [7] The trigger conditions herein are not indicative of appropriate trigger conditions for all devices. Appropriate trigger conditions may be more or less stringent. When trigger conditions used in testing differ from this table, the trigger conditions used must be defined in the test results.

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4.2.5 Record Keeping

Data shall be recorded for each pin failure and shall include the test condition (including clock frequency for dynamic devices, if used), vector set used for preconditioning, test temperature, trigger condition, and latch-up I_{SUPPLY} current. Data shall also be recorded for all pins and operating conditions that could not be completely tested per the JESD78 specification. This information shall identify the pins, operating states, and reason for incomplete testing.

4.2.5.1 Passing Level Results

If all device pins pass per the failure criteria requirements specified in Section 5 herein, then the following information shall be reported for each pin:

- a. Passing I-test current with applicable V_{CLAMP} value. If a voltage trigger (E-test) latch-up test is used, report the passing E-test voltage with applicable I_{CLAMP} value.
- b. Passing Overvoltage value for each independent V_{SUPPLY} pin (or pin group) with applicable I_{CLAMP} value.

4.2.5.2 Failing Level Results

If any device pins fail per the failure criteria requirements specified in Section 5 herein, then the following information shall be reported for each pin:

- a. Failing I-test current with applicable V_{CLAMP} value. If a voltage trigger (E-test) latch-up test is used, report the failing E-test voltage with applicable I_{CLAMP} value.
- b. Last passing I-test current with applicable V_{CLAMP} value. If a voltage trigger (E-test) latch-up test is used, report the last passing E-test voltage with applicable I_{CLAMP} value.
- c. Failing Overvoltage value for each independent V_{SUPPLY} pin (or pin group) with applicable I_{CLAMP} value.
- d. Last passing Overvoltage value for each independent V_{SUPPLY} pin (or pin group) with applicable I_{CLAMP} value.

5 Failure Criteria

A device failure is defined by any of the following conditions:

- a. Device does not pass the test requirements as stated below:
 1. Positive I-test current = $(I_{NOM} + 100 \text{ mA})$ or $1.5(I_{NOM})$ whichever is greater, with voltage clamped at 1.5 times maximum logic high or MSV whichever value provides maximum stress without creating an EOS condition.

Note: If E-test is used, positive E-test voltage = 1.5 times maximum logic high with current clamped at $(I_{NOM} + 100 \text{ mA})$ or $1.5(I_{NOM})$ whichever is greater. The trigger voltage for positive E-test is given by $V_{TRIGGER} = V_{MAX} + 0.5(V_{MAX} - V_{MIN})$ with an upper limit of $1.5(V_{MAX})$ where V_{MAX} (logic high) and V_{MIN} (logic low) are defined in JESD78 Section 2. If the Maximum Stress Voltage (MSV) for the pin (see Section 2 herein) is less than $V_{MAX} + 0.5(V_{MAX} - V_{MIN})$ or $1.5(V_{MAX})$ then the trigger voltage is given by $V_{TRIGGER} = MSV$.

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2. Negative I_{test} current = -100 mA or -0.5(I_{NOM}) whichever is greater in magnitude, with voltage clamped at -0.5 times maximum logic high or MSV whichever value provides maximum stress without creating an EOS condition. For VSS tolerant pins the voltage clamp must be set to -1.5 times minimum logic low.

Note: If E-test is used, negative E-test voltage = -0.5 times maximum logic high with current clamped at -100 mA or -0.5(I_{NOM}) whichever is greater in magnitude. The trigger voltage for negative E-test is given by $V_{TRIGGER} = V_{MIN} - 0.5(V_{MAX} - V_{MIN})$ with a lower limit of $-0.5(V_{MAX})$ where V_{MAX} (logic high) and V_{MIN} (logic low) are defined in JESD78 Section 2. If the Maximum Stress Voltage (MSV) for the pin (see Section 2 herein) is greater than $V_{MIN} - 0.5(V_{MAX} - V_{MIN})$ or $-0.5(V_{MAX})$ or $-1.5(V_{MIN})$ then the trigger voltage is given by $V_{TRIGGER} = MSV$.

3. V_{SUPPLY} Overvoltage test = 1.5(V_{MAX}) or MSV, whichever value provides maximum stress without creating an EOS condition.

- b. Device no longer meets the device specification requirements. Complete DC parametric and functional testing (initial and final ATE verification) shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Note: If an ATE verification failure is suspected to be caused by EOS damage during latch-up testing, adjust the trigger clamp level, repeat the latch-up test with new samples, and report test results as defined in Section 4.2.5 herein.

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Appendix A - Examples for Footnotes 2 & 4 (Table 2A)

Footnotes 2 and 4 of Table 2A are equations developed to handle products that have selected pins/functions that cannot operate below ground potential. The pins falling into this category generally are differential input pins but could be other functions.

A.1 Example 1: Standard Low Voltage Device

Power supply: 3.6 V

Ground: 0 V

Vmax:3.6 V (datasheet operating maximum for pin)

Vmin:0 V (datasheet operating minimum for pin)

Vclamp High = 3.6 V + 0.5*(3.6 V – 0 V) = 5.4 V (from Footnote 2 for Table 2A)

Vclamp Low = 0 V – 0.5*(3.6 V – 0V) = -1.8 V (from Footnote 4 for Table 2A)

A.2 Example 2: High Voltage Device

This device is from a high voltage (60V) DMOS process. This example describes an I/O pin.

Power Supply: $V_{DDNOM} = 60V$

$V_{DDMAXOP} = 66V$

Ground: $V_{SS} = 0V$

Minimum Breakdown of active devices (active transistors): $V_{BD} = 90V$ [N-Well / Psub]

MSV Characterization allows an MSV of 85V (margin of 5V) for this process

Vclamp High = 66V + (0.5)(66V – 0) = 99V

MSV = 85V (assuming $V_{SS} = 0V$)

Vclamp Low = 0V – (0.5)(66V – 0) = -33V

$V_{DDMAXOP} - MSV = -19V$

MSV limits the maximum clamp voltage to a spread of 85V in total I/O voltage to supply or ground resulting in the 85V [high voltage] and the -19V [low voltage.]

A.3 Example 3: VDD and VSS Tolerant I/O (Dual Polarity analog pin, MSV application specific)

Specification of a LIN- or CAN-driver of an automotive product. VBAT is supplied by the car battery, the analog I/O (LIN,CAN) needs to be tolerant to over voltage conditions in both directions. The analog I/O pin has an external pull up resistor to VBAT. Due to load dump and ground loss conditions, the pin must be tolerant to +40V and -27V (OEM requirements)

Power supply: 18 V with V_{ABSMAX} : 42 V(limited by external load dump protection diode)

Ground: 0 V

Minimum Breakdown of active devices (Process) $BV > 65 V$

High signal of analog I/O pin (LIN, CAN): 18V, $V_{ABSMAXIO}$: +40 V

Low signal of analog I/O pin (LIN,CAN): 0V, $V_{ABSMINIO}$: -27 V

Vclamp High I/O = 40 V + 0.5*(40 V +(-) 27 V) = 73,5 V; limited by 1.5* $V_{ABSMAXIO}$ to +60V

Vclamp Low I/O = -27 V – 0.5*(40 V +(-) 27 V) = -60.5V; limited by -1.5* $V_{ABSMINIO}$ to -40.5V

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A.4 Example 4: VDD tolerant I/O (MSV set by process limit)

Specification of an automotive product with the feature of an open drain output driver. VBAT is supplied by the car battery, the open drain output device must be tolerant to positive over voltage exceeding VBAT. Therefore it qualifies as a VDD tolerant I/O.

Power supply: 18 V with $V_{ABS\text{MAX}}$:42V

Ground: 0 V

High of open drain output pin: 12V with $V_{ABS\text{MAX}}$: 50 V

Low of open drain output pin: 0 V

$V_{ABS\text{MAX}}$ of any I/O pin is different than the $V_{ABS\text{MAX}}$ of Vsupply.

Minimum Breakdown of active devices (active transistors) $BV > 60 \text{ V}$ (process limit)

$V_{\text{clamp High I/O}} = 50 \text{ V} + 0.5 \cdot (50 \text{ V} - 0 \text{ V}) = 75 \text{ V}$; is beyond the process limits, MSV is set to 60V

$V_{\text{clamp Low I/O}} = 0 \text{ V} - 0.5 \cdot (50 \text{ V} - 0 \text{ V}) = -25\text{V}$; due to the presence of the low side diode the required forcing current will be reached well before the clamping voltage is reached, making the clamping voltage less relevant.

The positive current stress fails because the stress voltage increases up to 65V which exceeds the breakdown voltage of the process. Reducing the MSV to 55V which is still above the maximum available voltage during a transient disturbance leads to a pass and fulfills the specification. The negative stress is easily handled by the drain body diode of the output driver. The report must contain pin names with MSV values to which they were tested.

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Revision History

<u>Rev #</u>	<u>Date of change</u>	<u>Brief summary listing affected sections</u>
-	June 9, 1994	Initial Release
A	May 15, 1995	Added copyright statement. Revised the following: Foreword; Sections 2.3, 2.4, 3.1, 3.2, 3.4, 3.5 (g, h, l, o, and p), and 4.0; Tables 1 and 2; Figures 2, 3, and 4.
B	Sept. 6, 1996	Revised the following: Sections 1.3.1, 1.3.7, 1.3.8, 2.1, 2.3, 3.1, 3.2, 3.3, 3.4, 3.5 (o, p, and q), 4.0, and 5.0; Figures 1 and 4.
C	Oct. 8, 1998	Replaced CDF-AEC-Q100-004 with the JEDEC IC Latch-up Test specification EIA/JESD78 with additional requirements. Added the following requirements: Sections 1.2, 1.3, and 4.1 (to correspond with the JEDEC specification section numbers); Table 1A (E-test addendum to JEDEC specification Table 1).
<u>D</u>	<u>Aug. 7, 2012</u>	<u>Complete Revision. Revised Acknowledgement, Sections 1.1 and 4.1, and Table 2A. Added Notice Statement, reference to latest version of JESD78, Sections 2 (Maximum Stress Voltage, E-Test, VDD Tolerant I/O, and VSS Tolerant I/O), 4.2.5, 4.2.5.1, 4.2.5.2, and 5, Table 2A (footnotes 2 and 4), and Appendix A. Deleted signature block and Section 1.3.</u>