

ATTACHMENT 2

AEC - Q100-002 REV-E

HUMAN BODY MODEL ELECTROSTATIC DISCHARGE TEST

Automotive Electronics Council

Component Technical Committee

Acknowledgment

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Council would especially like to recognize the following significant contributors for the revision of this document:

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Change Notification

The following summary details the changes incorporated into AEC-Q100-002 Rev-E:

- **HBM stressing is now done in accordance with the ANSI/ESDA/JEDEC JS-001 specification. Any exception/addendum to this stress procedure is noted in Q100-002.**

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METHOD - 002

**HUMAN BODY MODEL (HBM)
ELECTROSTATIC DISCHARGE (ESD) TEST**

All HBM testing performed on Integrated Circuit Devices to be AEC Q100 qualified shall be compliant to the latest revision of the ANSI/ESDA/JEDEC JS-001 specification, with additional requirements as defined herein.

1.0 Tester Qualification (refer to JS-001 Section 5.3 “HBM Tester Qualification”)

1.1 An HBM tester used for AEC qualification shall meet the waveform requirements in JS-001 Table 1 for every voltage level of stress. The qualification or re-qualification shall be done according to JS 001 section 5.3, options a, b or c.

2.0 Test Fixture Board Qualification (refer to JS-001 Section 5.4 “Test Fixture Board Qualification for Socketed Testers”)

2.1 An HBM test fixture board used for AEC qualification shall meet the waveform requirements in JS-001 Table 1 for every voltage level of stress. The qualification shall be done upon initial acceptance of the test fixture board.

2.2 Re-qualification of the board shall be done after service or repair of the board after initial acceptance.

3.0 Device Stressing (refer to JS-001 Section 6.2 “Device Stressing”)

3.1 AEC HBM qualification testing shall be done at the following levels and skipping voltage levels is not allowed:

- a. 500 V, 1000 V and 2000 V
- b. If failures are observed at 500 V, HBM testing at 250 V shall be done. If failures are observed at 250 V, HBM testing at 125 V shall be done. If the device fails at 250 V and a tester that meets waveform requirements at 125 V is not available, the part shall be classified Class 0A (i.e., < 125 V).
- c. Voltage levels above 2000 V may be done for margin, higher threshold targets or high robustness characterization.

4.0 Pin Stress Combinations (refer to JS-001 Section 6.5 “Pin Stress Combinations”)

4.1 Devices with six (6) pins or less shall be tested with all possible pin pair combinations (one pin connected to terminal A, another pin connected to terminal B) regardless of pin name or function.

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4.2 HBM stress for AEC Q100 qualification shall be initially done using JS-001 Table 2B, with the following exceptions:

- a. HBM stress using a Low Parasitic Tester (LPT) (see Section 4.3 below)
- b. If a tester artifact is deemed to cause a false HBM failure, options contained within JS-001 Table 2A may be used.
- c. If a failure is deemed to be caused by cumulative stress, options contained within JS-001 Table 2A may be used.

4.3 AEC Q100 stress using a Low Parasitic Tester (LPT), such as a Two Pin HBM Tester.

- a. Connectivity for each stress combination shall be verified. Refer to JS-001 Section 5.6.2 (“Non-Relay Testers”).
- b. Stress may use the Non-Supply to Non-Supply stress method found in JS-001 Table 2A (i.e., Pin combination N+1).
- c. In addition to the Coupled Non-Supply Pin Pairs, adjacent Non-Supply pins on the die shall be stressed in two-pin mode.
- d. Options outlined in JS-001 Section 6.6 (“HBM Stressing with a Low Parasitic Simulator”) related to LPT HBM testers may be used.

5.0 Test Reporting

Upon completion of the required testing defined herein, a report of the testing performed and detailed results, as defined below, including any deviations, shall be submitted to the user upon request.

- a. Tester Details
 - Tester type (e.g., relay, non-relay, low parasitic, etc.)
 - Charge removal circuit (if applicable)
 - Parasitic mitigation (if applicable)
- b. Sample Details
 - Package configuration (e.g., pin count, lead form, etc.)
 - Sample sizes
- c. Test Details
 - Pin groupings (e.g., non-supply, supply, coupled pin pairs, etc.)
 - Stress voltage levels
 - Test/Pin partitioning (if applicable)
 - Stress pin combinations
 - Exceptions to any tests performed
 - Pin combinations
 - Stress polarities
 - Stress voltages
- d. Test Results
 - Summary of results

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Revision History

<u>Rev #</u>	<u>Date of Change</u>	<u>Brief summary listing affected sections</u>
-	June 9, 1994	Initial Release
A	May 15, 1995	Added copyright statement. Revised the following: Foreword; Sections 2.3, 2.4, 3.1, 3.2, 3.4, 3.5 (g, h, l, o, and p), and 4.0; Tables 1 and 2; Figures 2, 3, and 4.
B	Sept. 6, 1996	Revised the following: Sections 1.3.1, 1.3.7, 1.3.8, 2.1, 2.3, 3.1, 3.2, 3.3, 3.4, 3.5 (o, p, and q), 4.0, and 5.0; Figures 1 and 4.
C	Oct. 8, 1998	Revised the following: Sections 1.2, 2.1, 3.1, 3.5 (d, e, j, and k); Tables 1 and 2; Figure 1. Revision to section 3.5 (d, e, j, and k) reflects a change from three (3) ESD pulses with a one (1) second minimum delay between consecutive ESD pulses at each stress polarity to one (1) ESD pulse with a 500 millisecond minimum delay between consecutive ESD pulses. The use of three (3) ESD pulses with a one (1) second minimum delay between consecutive ESD pulses is also acceptable. Revision to Table 1 reflects a $\pm 10\%$ tolerance applied to all Ips (I _{peak} for short) parameter values.
D	July 18, 2003	Revision to sections 3.5 (p & q) and 5 reflect addition of classification levels for ESD testing and lower voltage step for devices failing 500V. New Table 3 added listing HBM ESD classification levels.
E	Aug. 20, 2013	Complete revision. Aligned the AEC HBM stress procedure to the ANSI/ESDA/JEDEC JS-001 stress method. Additional requirements for automotive qualifications are listed.