Basics of ATE Test

Revised 8/8/2007

Course Contents

1. Introduction to Semiconductor Testing

Design and manufacturing cycle of an IC
Semiconductor Companies/Staffs
ATE – Automated Test Equipment and its components
Load boards, Probe cards, Handlers, Probers

2. Project Plan, Specifications and Test Program

Project/Test Plan – Introduction, Benefits, Requirement, Sample
Specifications – Design, Test, Device, Sample
Test Program – Types, Consideration, Test Flow, Binning, Summary
Common Categories of Test for Semiconductor Device
Functional, DC, AC Specifications of Device

Course Contents

3. DC Parameters Test (including Continuity Test)

Continuity Test - Concept, Test Method, Sample Datalog

DC Tests – Concept and Test Method

- Power Supply Current Test (IDD)
- Leakage Test (IIL/IIH)
- IOZL/IOZH, IOS
- VOL/IOL, VOH/IOH

ATE DC Subsystem - VI Source, DC Meter, DC Matrix, Relay Control

4. Digital Functional Test

ATE Pin Electronics

Test Concepts – Pattern, Timing, Levels

IO Signals – Input Signal Generation, Output Signal Compare

Functional Testing Basic – Example VIL/VIH, VOL/VOH

Test Vectors

Course Contents

5. AC Parameters Test

AC Timing Tests - Setup Time, Hold Time, Propagation Delay, etc
ATE Time Measurement Subsystem
Timing Calibration

6. Introduction to Mixed Signal Testing

Sampling Theory – Nyquist Theorem, Coherency Formula
Fast Fourier Transform (FFT) – Frequency Domain Analysis
Generic Mixed Signal Tester Architecture – AWG and Digitizer

7. ADC and DAC Test

ADC and DAC Basic
Static Test – Histogram method (INL, DNL)
Dynamic Test – SNR, THD, SINAD

Course Contents

8. Debug Tools and Debugging

Tools - Datalog, Histogram, Shmoo, Pattern Debugger, Waveform Tool

Trouble-Shooting Techniques

9. Introduction to Design-For-Testability

DFT consideration

Test Approach – AdHoc, Scan (and Boundary Scan), Self-Test (BIST)

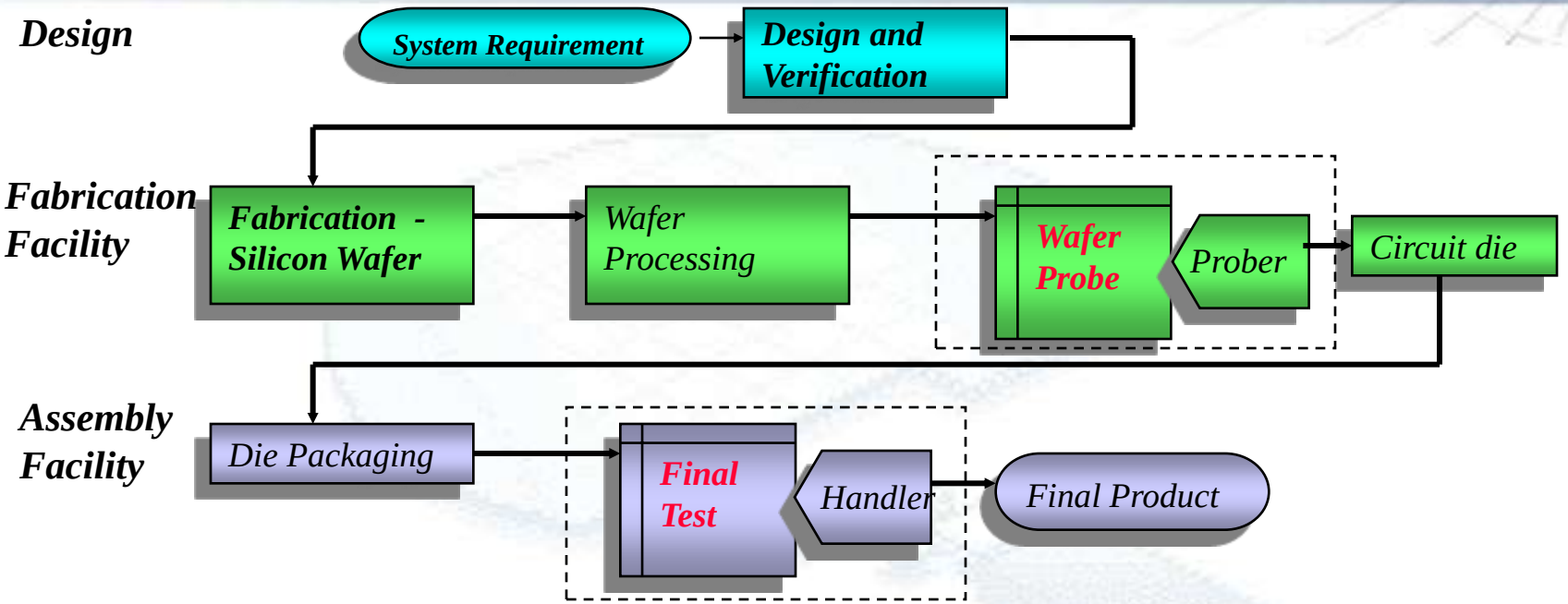
INTRODUCTION TO SEMICONDUCTOR TESTING

Revised 8/8/2007

Overview

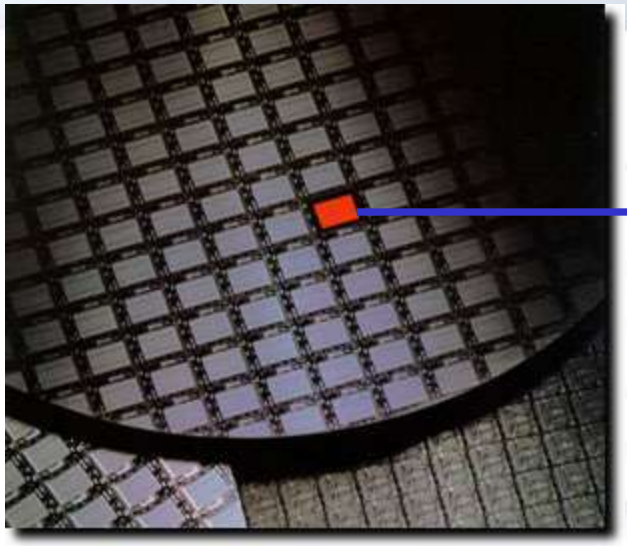
- Design and manufacture cycle of an IC
- Classification of IC`s
- What is ATE ?
- Why tester ?
- What is test ?
- Components of a Test System
- Load boards /Probe cards
- Typical Test program flow
- Handlers /Probers

IC Design & Manufacturing Cycle

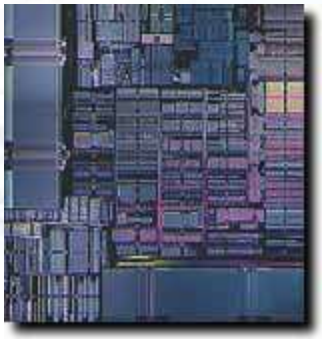


- Devices are tested at two points:
  - **Wafer Probe** – In this the die on the wafers are tested using very fine needle like probes. The equipment that interfaces with the ATE at this stage is called a Prober.
  - **Final Test** (or Assembly Test or Package Test) – At this stage the devices are in packaged form (called chips). Machines used to interface package parts to the ATE are called Handlers

Wafer, Single Die and Package device



Wafer



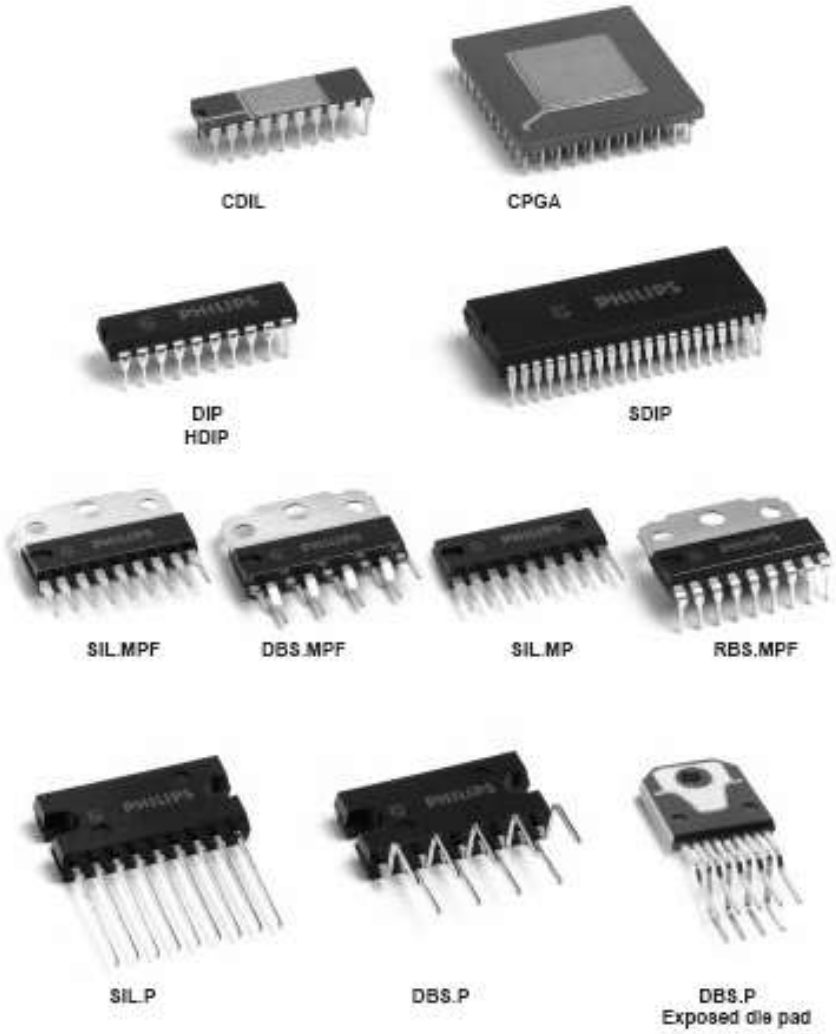
64-Bit RISC
Microprocessor Die
(Motorola)

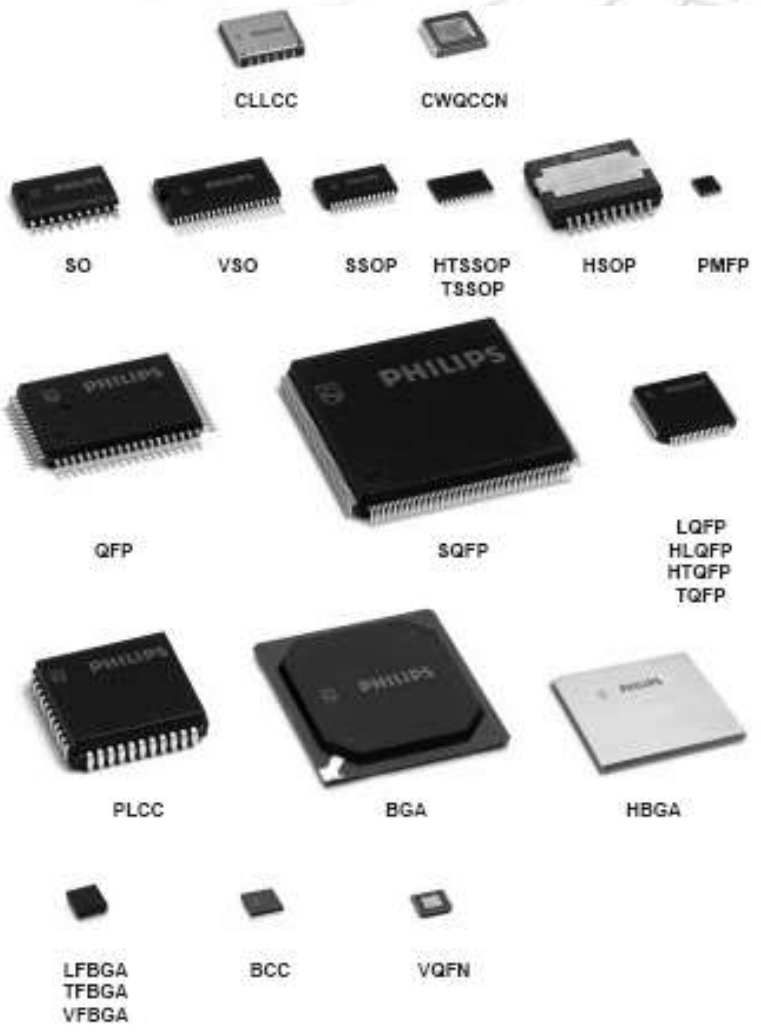
Die

DIP (Dual Inline Package) Device
(AMD Corporation)

Package Device

Standard Packages





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Classification of IC`s

- **Digital IC**

  A digital integrated circuit uses digital signaling and is the most popular type of IC. For example a microprocessor IC.

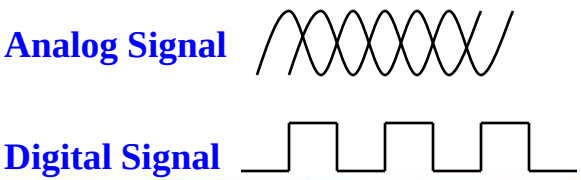
- **Analog or Linear IC**

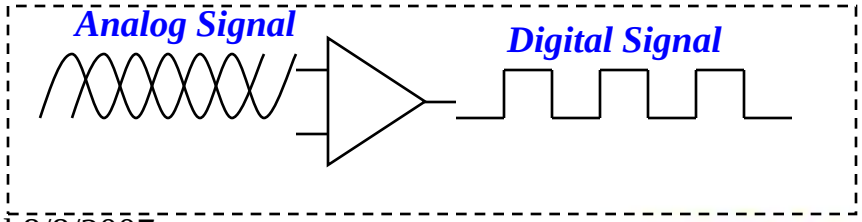
  An analog integrated circuit contains no digital data path control functions. All signals are analog. For example an audio amplifier IC.

- **Mixed Signal IC**

  A mixed signal IC contains both analog and digital components. It is the fastest growing segment of the industry. For example a single chip radio IC,ADC,DAC.

  To minimize cost and size of the end product, more and more functions are being integrated on a single chip and such devices are referred to as System-On-Chip or SoC devices.





Semiconductor Test Companies

- **Integrated Device Manufacturer (IDM):** Semiconductor companies that have integrated operations including design and manufacturing. *Examples: IBM, Intel, Texas Instruments, Samsung, STMicroelectronics*
- **Strategic Outsourcing Model:** A newly adopted business model that allows IDMs to outsource leading edge designs, while maintaining process technology development. *Examples: Motorola and ADI*
- **Fabless:** A business model whereby a semiconductor company outsources at least 75 percent of their silicon wafer production to outside sources. *Examples: Qualcomm, Broadcom, Marvell, Nvidia*
- **Foundries:** A silicon wafer manufacturer that partners with companies to manufacturer their silicon wafers. *Examples: TSMC, UMC, Chartered, SMIC, Silterra, 1st Silicon, IBM Microelectronics*
- **Sub-Contractors (SubCon):** Companies that provide manufacturing services on Wafer Testing, Die Assembly, Packaged IC Testing to other semiconductor companies. *Examples: ASE, Amkor, SPIL, StatsChipPAC, KYEC, UTAC*

Test Related Personnel

- Test engineers
  - Write & debug test programs, correlate with bench (evaluation boards)
- Product engineers
  - Monitor the product, set test limits, diagnose failures
- Shop operators
  - Organize product through the shop floor
- Applications engineers
  - Help with testing situations, software bugs, new features, give presentations
- Maintenance staff
  - Keep machines alive !!
- Field service
  - Vendor staff who install new machines, and fix tricky problems

Common ATE Buzz Words

ASP - Average Selling Price

ATE - Automatic Test Equipment

DUT - Device Under Test

DIB - Device Interface Board - or LOAD board

DIE - An individual site on a wafer

HIB - Handler Interface Board - another name for the DIB !!!

PIB - Probe Interface Board - used with wafer probing

PROBE CARD – PCB with needle-like probes used at wafer probing

BINNING - Sorting the DUTs dependant upon test results

MANIPULATOR - Structure that supports the test head and allows it to move in many directions. This movement allows it to access other pieces of equipment.

HANDLER - Mechanical assembly for placing DUTs in the test head socket

PROBER - Mechanical unit for moving the wafer under the test probes

What is ATE ?

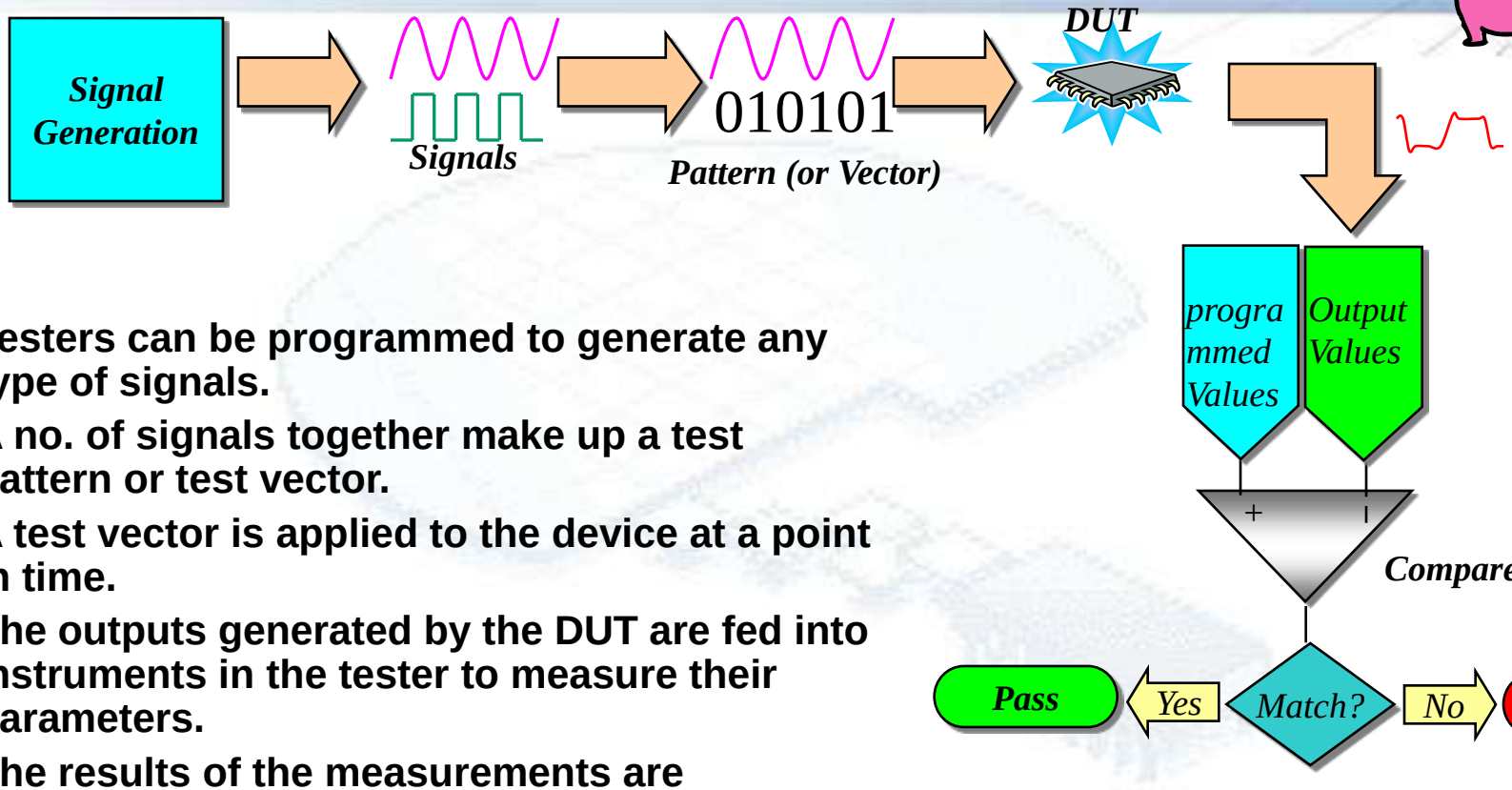
- ATE is a collection of high performance computer controlled test instruments.
- Automated test systems encompass a broad range of such instruments controlled by a computer . Each system includes all the equipments used to test a semiconductor device's functionality.
- Test program tester computer controls the test hardware by executing a set of instructions called test program .
- Testers ensure the integrity, quality and reliability of semiconductor components.
- Testers consist of electronic systems that generate signals, establish appropriate test patterns, properly set them in sequence and then use them to drive the semiconductor device itself.

Why Tester ?

Testing Large no. of devices → More Profitability

- Testers help in automating this task so that it can be done at a high speed without compromising on the accuracy of the test.
- The same tester can be used to test a wide variety of devices reducing the overall impact of the capital investment required to utilize a tester.
- Testers help in achieving a shorter “Time to Market”
- Testers help in achieving repeatable accuracy & correlation of results

How Does Test System Work ?



- Testers can be programmed to generate any type of signals.
- A no. of signals together make up a test pattern or test vector.
- A test vector is applied to the device at a point in time.
- The outputs generated by the DUT are fed into instruments in the tester to measure their parameters.
- The results of the measurements are compared to “programmed Values” stored in the ATE.
- A device is considered functional if the measured parameters match the programmed/golden values within acceptable tolerances

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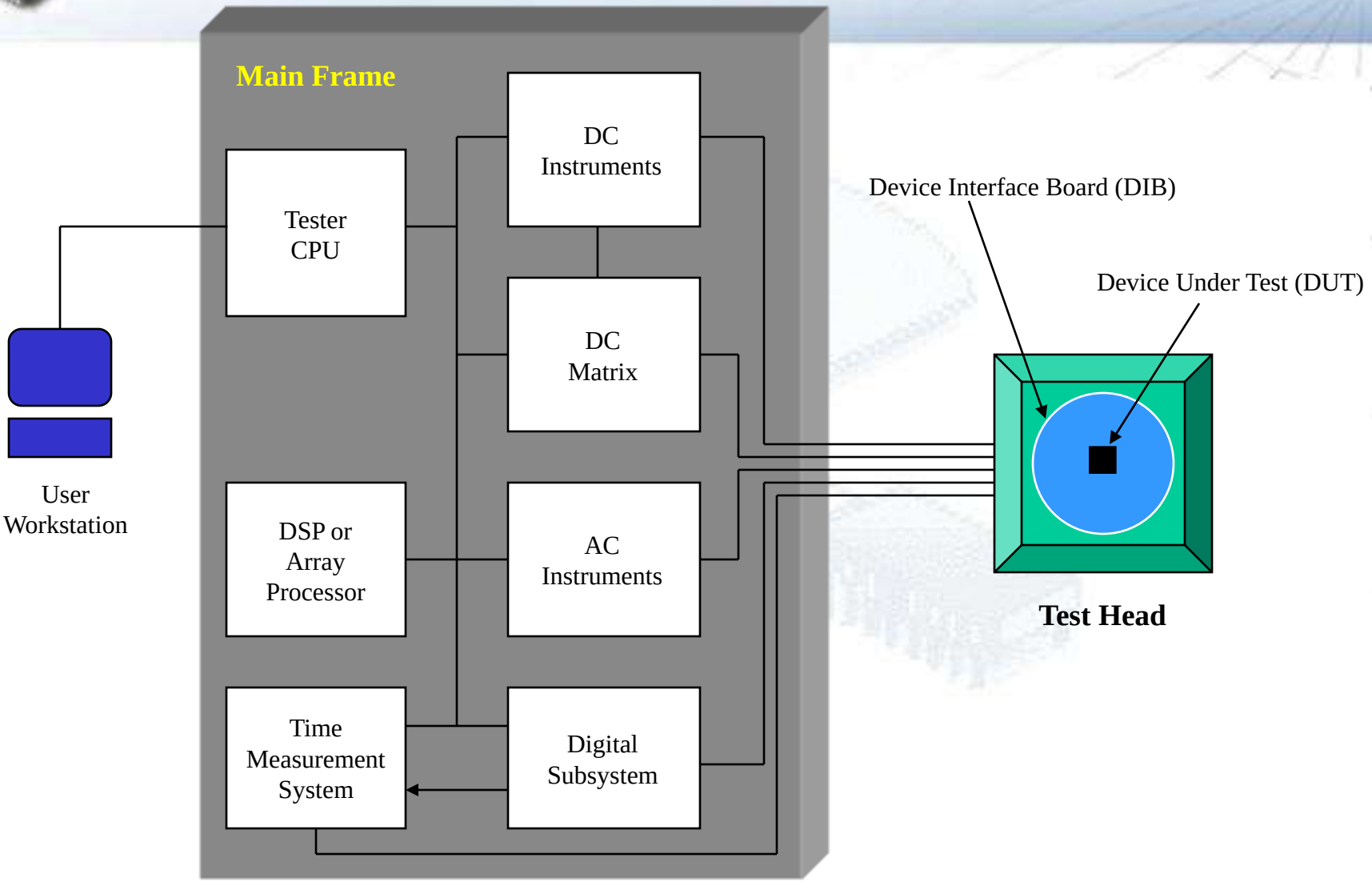
ATE Machine Types

- VLSI Testers
  - Period based, Number and Speed of Pins, Signal Integrity.
- Memory Testers
  - Similar to VLSI tester with Memory Test Pattern Generation and good Multi-Site capability.
- Mixed-Signal Testers
  - Frequency Based, Digital and Analog highly synchronized, Multi-Site capability.
- RF Testers
  - RF Generators, RF Ports, Network Analyzers
- Power Testers
  - High Voltages and High Current Switching
- SystemOnChip (SOC) Testers
  - Can do it all !!! (Big Advantages)

Mixed Signal Test System



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Mixed-Signal: Tester Requirements

Digital	Sequence Control Clock data Digital pattern Pins Serial I/O
DC Instruments	Power Supplies DC Matrix DC meter
AC Instruments	Arbitrary Waveform Generator Digitizers Video Instruments Time Measurement
DSP Processing	Digital Signal I/O Array Processing Synchronization

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Major Test System Elements

Tester MainFrame

To house test instruments, system support instruments (CDU, DSP Processor)

Tester TestHead

House test instruments channels that interface onto DIB.

User Workstation And/Or Tester Computer

For user to load/debug/execute test programs, process, datalog and store test results

Manipulator

Support structure that enables TestHead to move and dock to handler/prober

DIB (Device Interface Board)

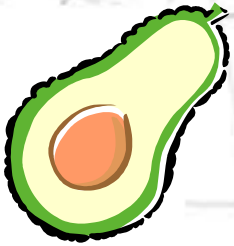
Hold test socket for device, or for interface with probe card.

Handler/Prober

Mechanical Equipment to enable device/wafer to be positioned for testing/probing

Components of a Test System

Typical components of a tester.



- Test head
- User/Tester computer
- DC subsystem
- Digital subsystem
- AC subsystem
- Time measurement system
- Channel card electronics
- Timing and formatting Electronics
- Power subsystem to provide adequate stable power to all of the above.

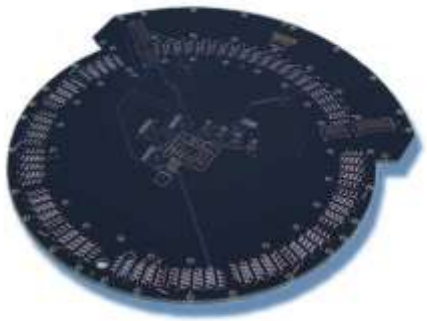
Load Boards/ DIB Boards

A **Load board** or DUT board is a circuit board designed to serve as an 'interface' board between the automatic test equipment (ATE) and the device under test (DUT) for packaged devices.

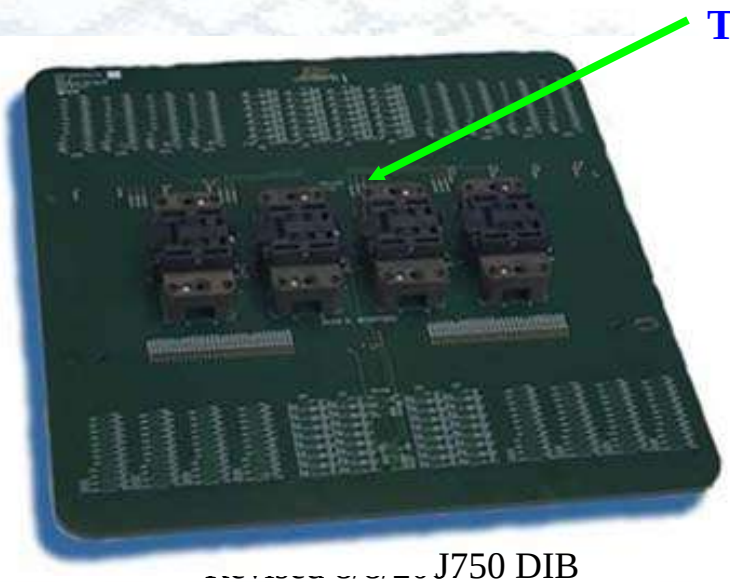
Load boards contain the necessary components to:

1) Set up the DUT for correct testing by the ATE.
2) Route the test and response signals between the DUT and the ATE.
3) Provide additional test capabilities that the ATE may not be able to provide.

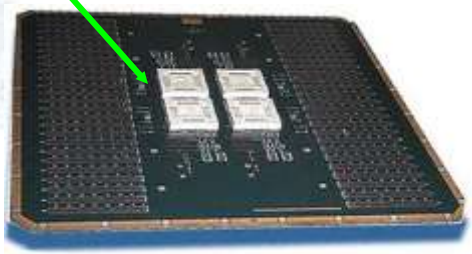
There are also load boards designed for the purpose of testing or calibrating the ATE itself.



Catalyst DIB



J750 DIB

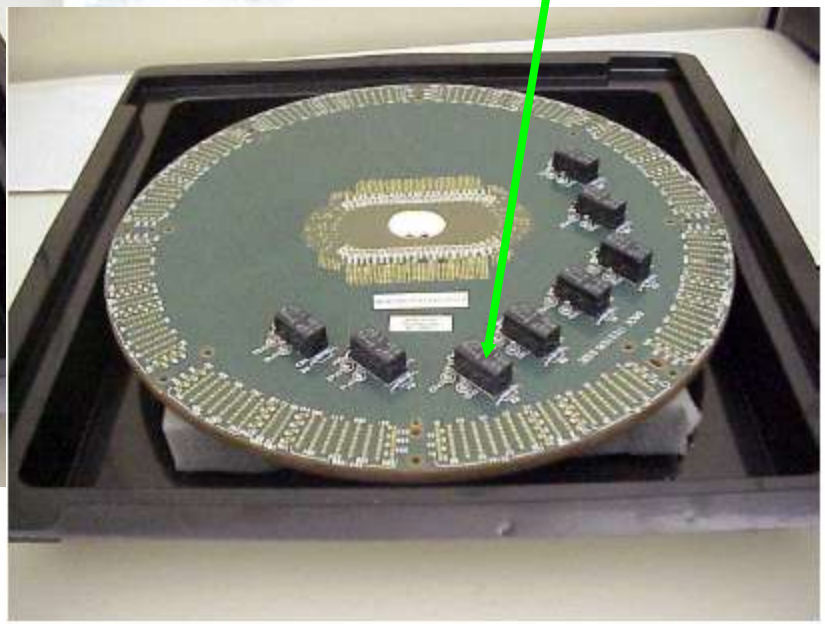


Flex DIB

Probe card

A **Probe card** is a circuit board designed to serve as an 'interface' board between the automatic test equipment (ATE) and the Die under test (DUT) for wafer probing.

Probe cards connect the test head electronics to individual pads of the die.



Relays and external components

Probe pins

Handlers

What is a handler ?

A handler is a complex machine that moves the packaged device to the tester so that it can be tested.

Who makes handlers?

Synax
MultiTest
MCT
ASECO
EPSON.. etc

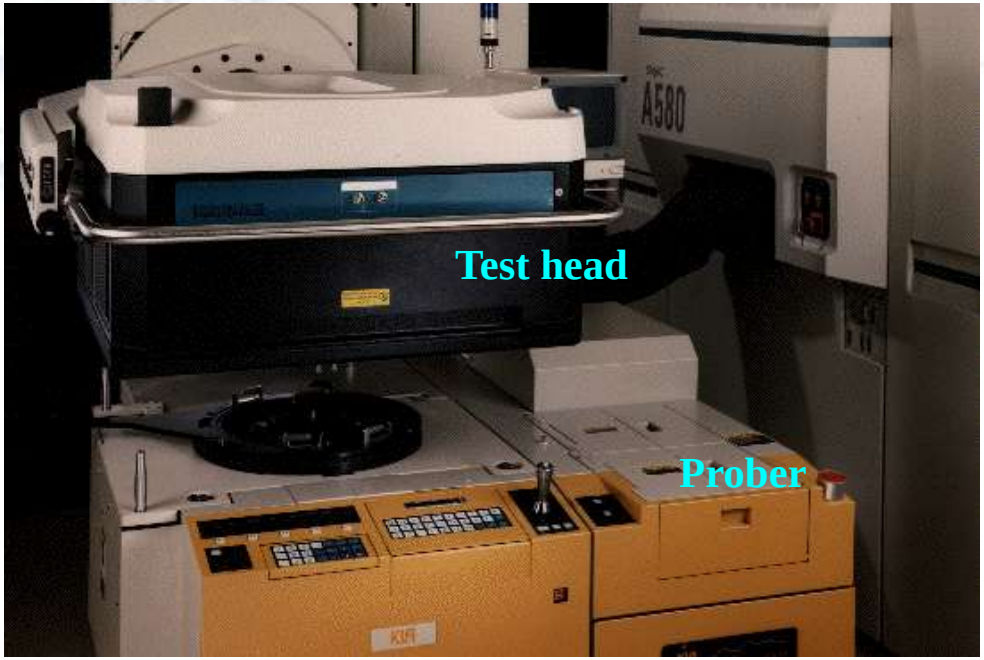
Probers

What is a Prober ?

A Prober is a complex machines that moves the whole wafer (unpackaged devices) so that it can be tested.

Who makes Probers?

TEL
Electroglass
TSK …etc



Self-Assess Questions

1. Which of the below are the elements of a test systems?
   Tester, Handler, Prober, Manipulator, Loadboard

2. Which of the below are not part of an ATE tester?
   Mainframe, Manipulator, Loadboard, User Workstation, Handler

3. What do the below acronyms stand for?
   ATE
   DIB
   DUT
   SOC

4. In IC Manufacturing cycle, testing for the IC functionality is performed at 2 stages. One is Final/Package Test. What is the other?

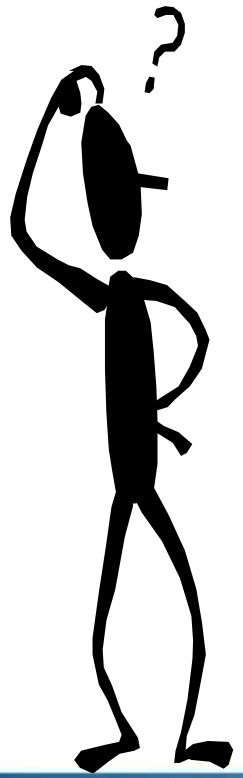
5. Name at least 2 categories/classification of IC Device

PROJECT PLAN , SPECIFICATIONS, AND TEST PROGRAM

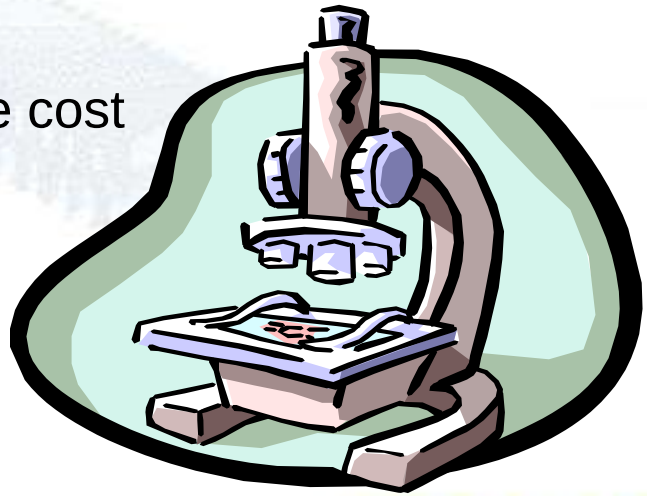
WHAT IS TESTING ?

Testing is the process of sorting the defective from non-defective, segregating bad and good units.

We do testing to



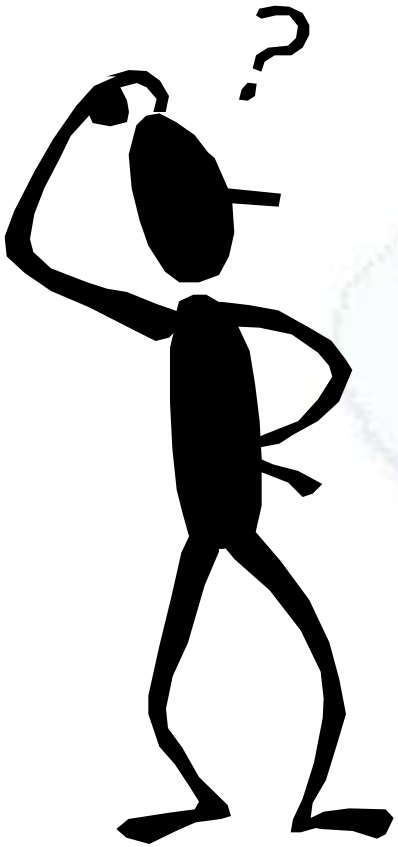
- Ensure quality product
  - Meet published device specifications
  - Characterize to determine device performance and provide design feedback
- Detect faults at earlier stage to save cost
- Provide feedback on process



What is Project Plan ?

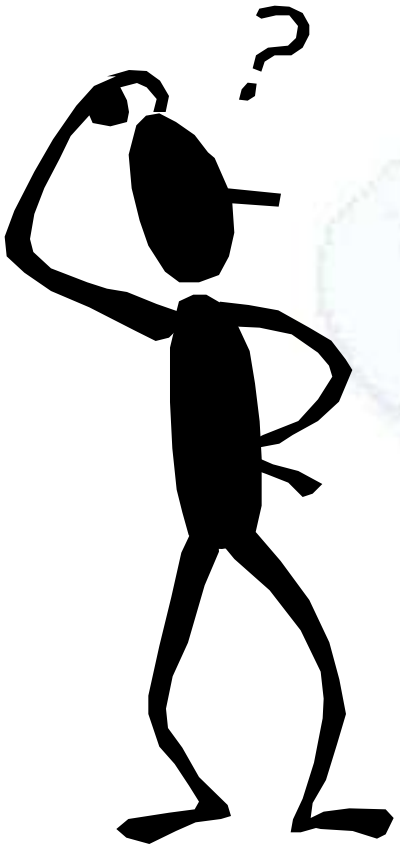
- Formal documentation of test goals and procedures.
- An iterative planning process using all available data.

Why do we need Project Plan?



- To define goal, scope, requirements, schedule, cost, resources, timeline, expected performance and confidence level.
- To measure the progress of testing activities by comparing actual performance against expected performance.

Benefits of having a Project Plan?



- Specify what activities to be part of testing process
- Improve communication among individuals (engineers)
- Reduce chance of failure during the execution of the test

What If We Don't Have Project Plan?

"We just don't have time to do an adequate job for testing."

What If We Don't Have Project Plan?

*"Most of the **costs** associated with testing are incurred because we enter testing without a **clear idea** of what is to be accomplished and how it is to be accomplished."*

When do we start generating Project Plan?

- As soon as the project's requirements are defined.

Requirements for a Project Plan

Some basic knowledge required to generate test plan are as follow:

I. DUT Requirements

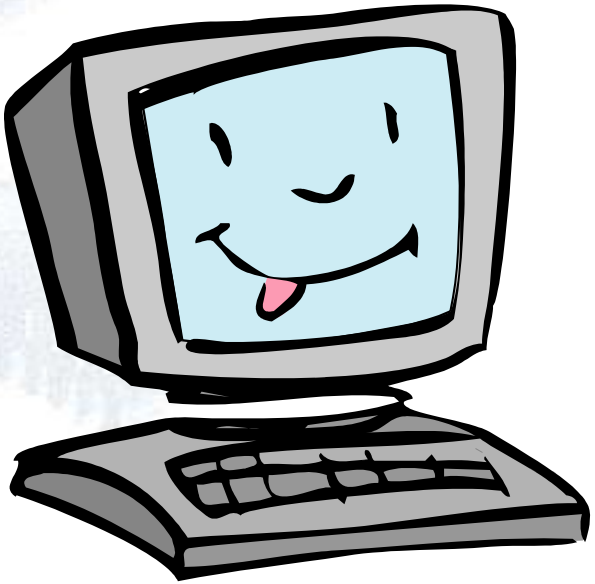
II. Tester

III. DUT Interface

IV. Software Environment

V. Device Test Plan

VI. Project Gantt Chart



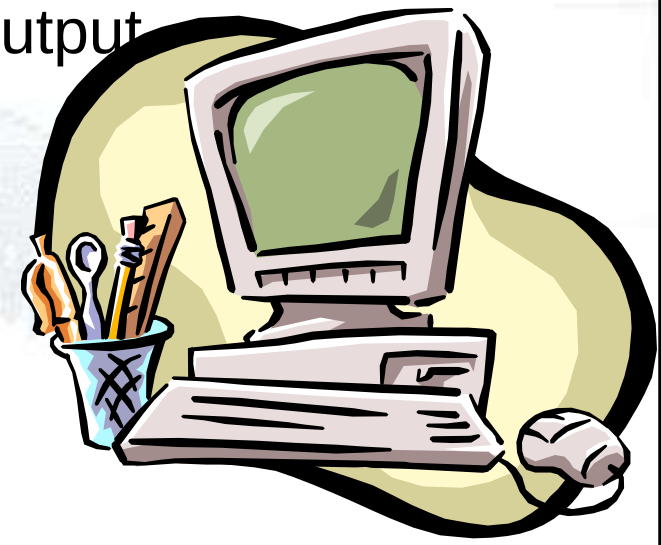
Device Testing Requirement

I. DUT Requirements

- Description of each pin
- Details of parameters to be tested
- DC & AC specifications of the device , etc
- Signals Requirements for input/output

II. Tester

- Availability of instruments
- Accuracy of instruments
- Programmability of instrument
- Specification Manual



Device Testing Requirement

III. DUT Interface

- The purpose is to connect the DUT pins to the system to send and receive signals.

- DIB is the hardware interface between the DUT and the tester .

IV. Software Environment

- Software to generate and run the test program

- At the end, the test results are recorded and the binning result sent to the operator

Device Testing Requirement

V. Device Test Plan

This is a documentation of the detailed description of all the tests in the Test List with binning information.

IV. Project Gantt Chart

A chart showing the scheduling Plan of the project phases.

Device Test Plan Sample

Test Plan for XXXX Device

Binning info

Test #	Description	Binning
	Basic Functional Test VIL=0.8V, VIH=2.0V, VOL=0.45, VOH=2.4V SPEED = 1MHZ Pattern Used: Func1_pat	
30	At Vccnom	10 FAIL
40	At Vccmin	
50	At Vccmax	

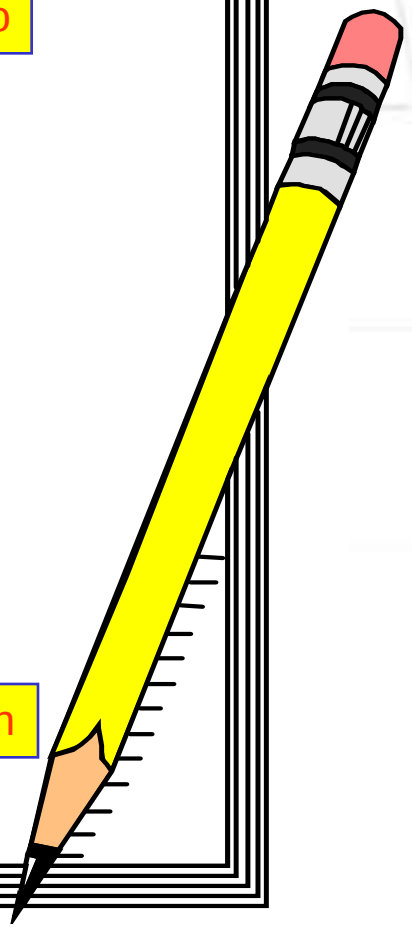
Test number

Test conditions

Test Description;

The functional tests did a write of 1010 to ports 4-7 follows by a read of 0101 from ports 4-7 at Vcc= min, max and nom.

Test description



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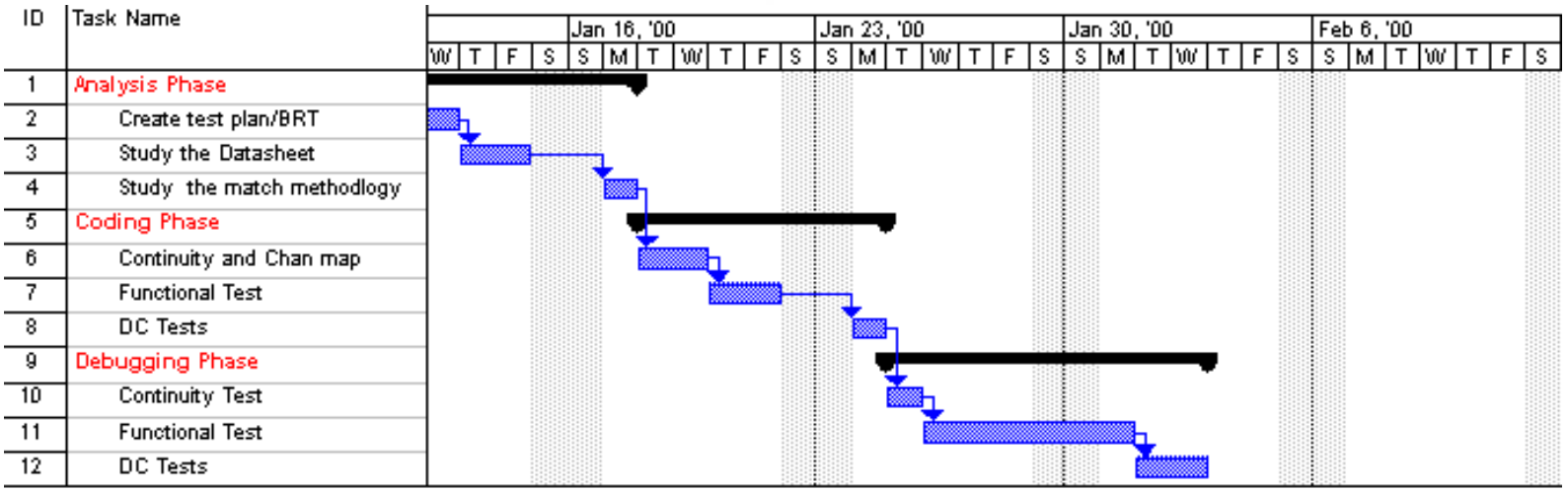
Sample Gantt Chart



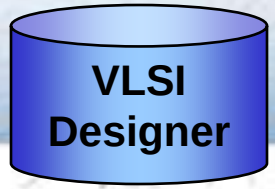
Requirement to Create a Test Program

- To generate a test plan, details of the device specification should be reviewed
- Test specifications and tests to be executed need to be prepared.
- Test hardware (Load board and probe card) need to be designed accordingly
- Test program need to be generated based on the test plan

Specifications - Overview

- Design specification
- Test specification
- General test methods
- Device specification
- Sample specification

Design Specification

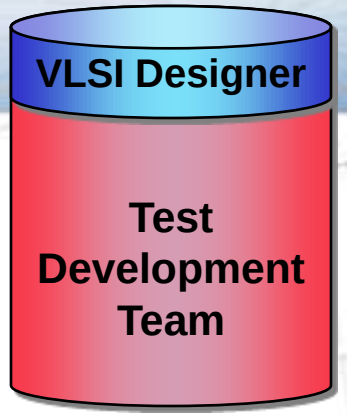


- Design Specification is a document which contains the definition of intended functions and performance characteristics of a new circuit design

- Design specification will be mostly created by Sales/Marketing dept or design engineering dept. In some cases it will be created by end user also.

- After producing the device it must be characterized and the actual performance of the device will be compared with Design Specification.

Test Specification



- Test Specification is a document which contains the detailed step-by-step procedure to test the circuit fully
- Test specification will be created by combined effort of design, test and product engineering departments.
- It defines the exact conditions to be used for Test Program development
- While testing, if there is any difference in any parameter, it will be noted and updated in the published device specification.

Device Specification

*** will be covered in more details in next chapter**

- Device specification is a published document by device manufacturer. It is called Datasheet or Data book specification.
- It contains the general current, voltage and timing details of the device which will be used for Test program development.

PARAMETER	TEST CONDITIONS‡			SN5400			SN7400			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −12 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = 0.8 V,	I_{OH} = −0.4 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.4 V				40			40	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				−1.6			−1.6	mA
I_{OS}¶	V_{CC} = MAX			−20		−55	−18		−55	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			4	8		4	8	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			12	22		12	22	mA

To generate a good test plan?

- ☑ Study device specification !!

A test program manipulates tester machinery to

1. Simulate the operating environment of a DUT
2. Control the DUT to execute its operational functions
3. Measures its response and
4. Interprets the results to determine if DUT is good or bad

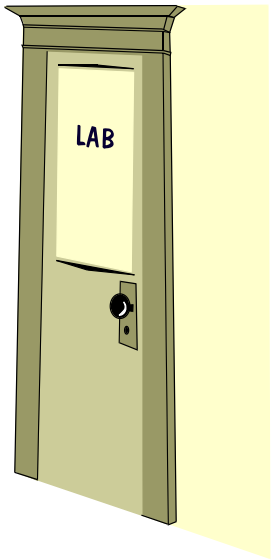
Types of Test Program

Test Programs are divided as follows.

a) Engineering
b) Characterization
c) Production

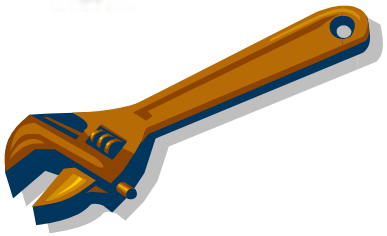
Engineering Test Program

- Initial test program is called as Engineering program which will be used to verify the functionality of the device.
- Should be flexible for altering voltages, currents and timings.
- Quick debugging & some characterization routines should be available.



Characterization Test program

- Extension of Engineering test program.
- Used to determine the operating limits.
- Tester pre-defined routines should be used to plot the characterization chart for shmoo, level search and time search routines.
- Usually after design, Characterization program is used to completely check if the device meets its specifications and collect characterization data.



Production Test Program

- Used to identify the bad devices from the good devices.
- It will be used for wafer sort, final test or QA test.
- Should be faster.
- Should be able to segregate failures and plot the summarized report (Yield).

Program Development Consideration

a) Hardware Limitations
b) Throughput
c) System Availability
d) Test Costs vs. DUT Cost

Hardware Limitations

- Test Specification should be reviewed and timing diagram should be developed to confirm the tester capability respective to test requirements.
- Test rate, voltage and current requirements should be accounted.
- Consider wafer probers, handlers and other external equipments.

Throughput & System Availability

- Estimation of test time in the target test system
- If the throughput is less, try for alternative test system.
- Availability of test system.
- Availability of support equipments.

Test Costs vs. DUT Cost

- Cost of the test device should be considered while selecting the target test system.
- If we use expensive test system for a low cost device, it will be less profitable to manufacture.

Creating a Test Program

- **Product Data Sheet**

  Contains Pinout , Functional details , DC & AC specification of the product.

- **Test Plan Matrix**

  Includes the exact test condition on all device pins,while performing each test.

Creating a Test Program

- **Tester Resources**

  Identify required resources within the tester which is capable of testing the product.

- **Load board Design**

  PCB where tester resources are wired to edge connector of the DUT directly or through some active/passive components.

- **Writing Test Program**

  Software coding which forces and measures required parameter in corresponding test platform.

Program Flow

- Test program flow is important for a production test .
- It is the sequence at which the test program is executed.
- Most fail tests should be there as firsts in flow.
- Throughput is very important factor in program flow.
- Test procedure for speed grading or multipass binning will give added advantage.
- Test summaries should be reviewed in period of time and flow should be modified if necessary.

TYPICAL TEST PROGRAM FLOW

- **Contact** (for open & shorts, DUT unpowered)
  - Check each DUT pin is connected - save failures for retest.
  - Uses the ESD diodes on the pins - usually test both diodes Vdd and Gnd.

- **DC Parametric Tests** (with DUT power applied)
  - Verifies the device DC (current, voltage) parameters

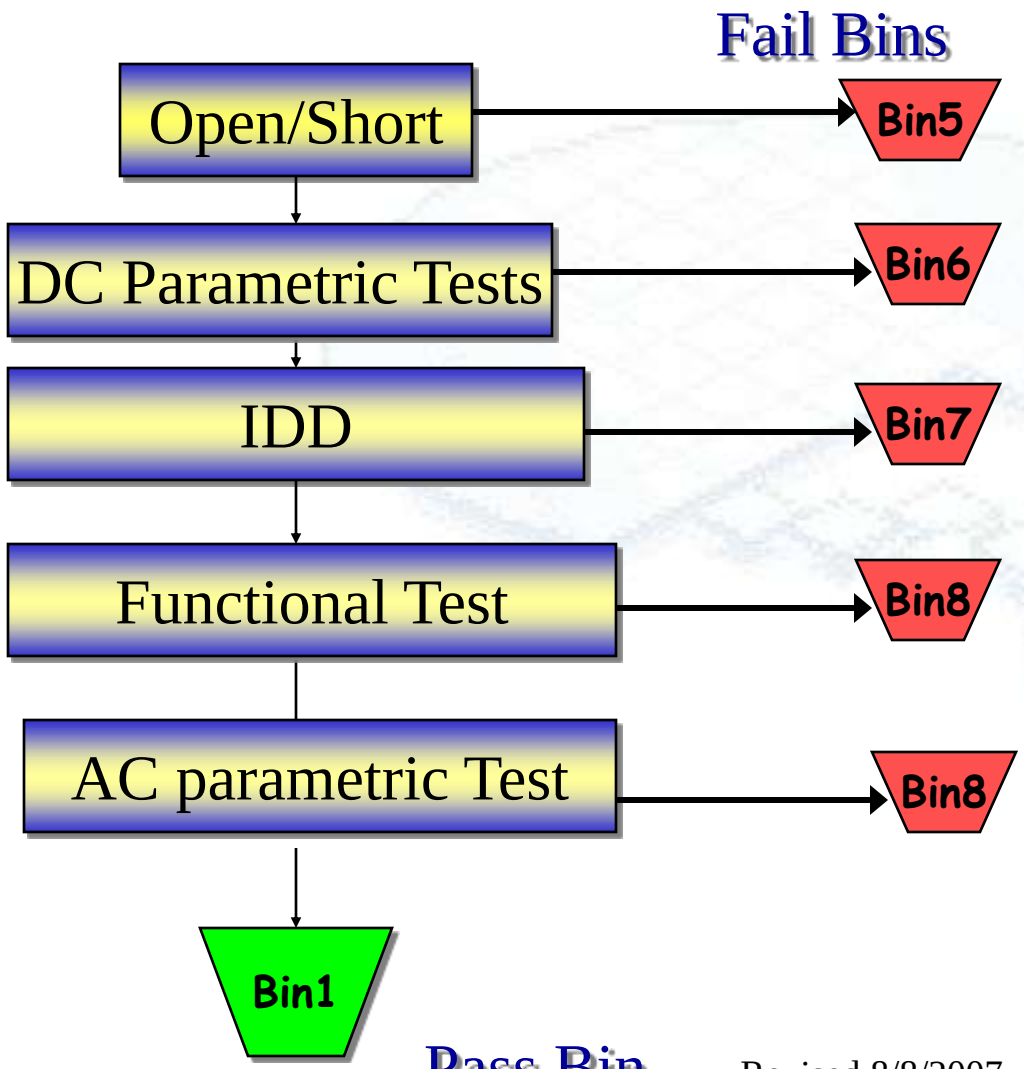
- **IDD/Power Supply**
  - Good indication of overall device functionality
  - Check during an operating mode

- **Functional tests**
  - Test out device for full functionality
  - May do a “quick functional” test first

- **AC Parametric tests**
  - Verifies the AC Specifications - includes quality of output signal and signal timing parameters

- **Binning**
  - May have several “good” bins - “Bin 1 is golden”, “happiness is bin 1”
  - Bin contact failures separately
  - Sometimes use bin numbers for ease of failure analysis.

Program Flow Diagram



This is a Typical test Flow with the binning details for the PASS and FAIL bins.

Program Initialization

- Test options (Wafer sort, final test, QA test, etc) should be selected by user.
- Additional information like Lot number, Operator ID and Test System number can also be provided.
- Instruction to setup the hardware may be provided in the opening menu for operator

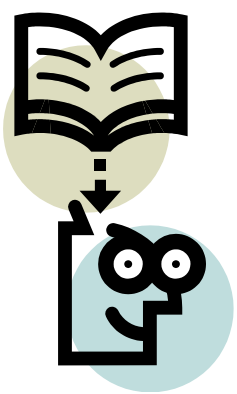
Test Setup Verification

- Load board check should be there.
- Quick diagnostic should be used to check the test system.
- Automatic load board identification should be possible.

Power-On Sequence

- Care must be taken for CMOS devices to avoid latch up.
- Latch up can cause excessive currents in flow within the device.
- Device powering up should be followed as per the Power On Sequence flow.

Power-On Sequence Flow



Power up VDD

Power up I/P Levels

Power up O/P Loading

Power up External HW

Device fully powered

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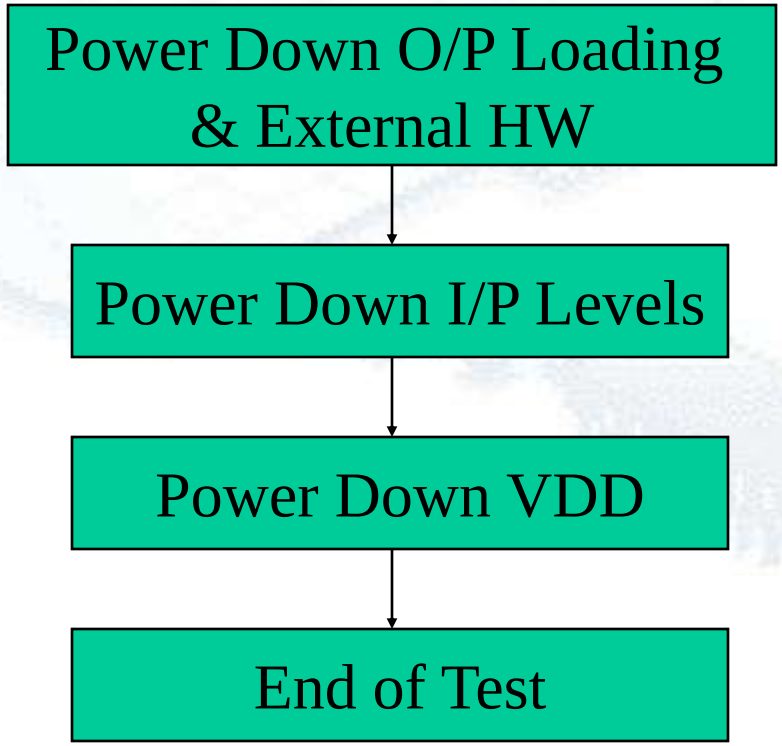
Power-Off Sequence

- Test System must be prepared for power down after binning is completed.
- VDD Supply should be the last one in powering down.
- Device powering down should be followed as per the Power Down Sequence flow.

Power-Off Sequence Flow



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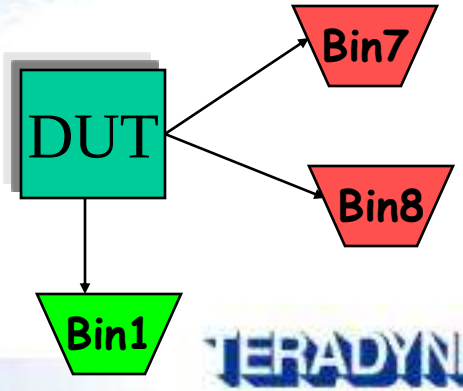
What is Binning ?

- Used for categorizing the tested devices.
- Binning is divided as *hard binning* and *soft binning*.
- Hard binning controls the physical operation where the DUT should be placed (tube or tray).
- Number of hard bins are limited by external handler whereas soft bins are unlimited which used to track various pass / fail categories.



Binning Cont …

A bin number is a number which represents the ultimate rating and performance of the DUT.

After a device is tested in final test, it is physically moved by the handler to the bin in which it belongs.

The bin number encompasses the gross characteristics of a device.

- **Hardware bins** are used by the attached handler or prober .
- **Software bins** can be used by the Test Engineer to group failure modes

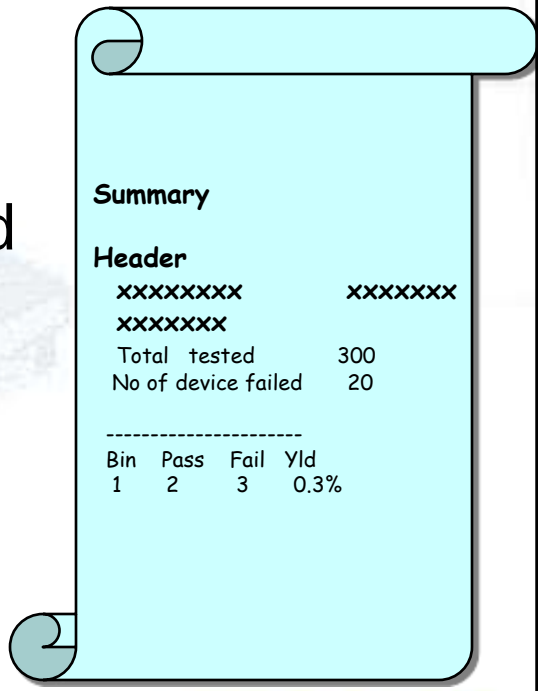
Binning Cont …

Sample binning

Hard Bin	Soft bin	#Category
1	10	Good Device
2	20	Opens and shorts reject
3	30	Gross Function fail reject
4	40	Functional VIL/VIH reject
4	50	Leakage reject
6	60	AC test reject
7	70	IDD test reject

Test Summary

- Test summary provides statistical information.
- Summary should indicate total tested, total passing /failing and the number of failures in each category.
- Test summary gives valuable input for yield issues, so it should include more information in it.
- Partial summary should be able to be produced during production testing.



Sample Test Summary

**********SUMMARY REPORT**********

TEST TEMP: 85C LOT NUMBER: 123568 01/23 DATE 24 FEB 2004

TOTAL UNITS TESTED : 1000
TOTAL GOOD UNITS : 800

****

	TOTAL UNITS	% OF TOTAL
TOTAL TESTED	1000	
TOTAL PASSED.BIN 1	300	30
TOTAL PASSED.BIN2	500	50
TOTAL FAILED	200	20
Cont_dym_Short	10	1
Cont_dym_Open	00	0
Cont_Parametric	00	0
Functional_Test	30	3
Low_Leakage_Test	30	3
High_Leakage_Test	00	0
TristateLow_Leakage	10	1
Static_Icc	50	5
Dynamic_Icc	50	5
Freq_counter_Test	20	2
Scan_Test1	00	0
Falltime	00	0
Falltime_meas	00	0

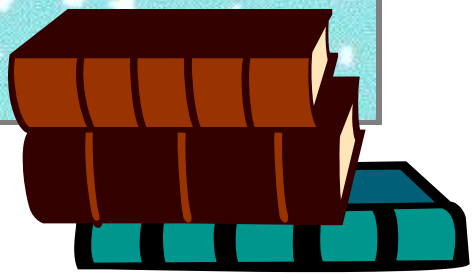
Total devices : 1000 Total passed devices : 800 Total

****

Test Program

What we have learnt:

- Types of test program
- Consideration in Program Development
- Typical production test program flow
- Program flow
- Power on/off sequence
- Binning
- Test summary



COMMON CATEGORIES OF TEST

Contact/Continuity Test

Checks for open circuits or short circuits in the device pins

DC PARAMETRICS TEST (including IDD)

Verifies the device DC current and voltage parameters

DIGITAL FUNCTIONAL TEST

Tests the logical operations of the DUT

AC TIMING TEST

Verifies the AC specifications which includes quality of output signal and signal timing parameters

MIXED SIGNAL TEST

Verifies operations on analog and digital circuitries of the DUT

DC Parametric Testing

a) Testing Input Voltages and currents
b) Testing Output Voltages and currents
c) Power Supply currents and voltages
d) Pass/fail limits for each parameter

Some DC PARAMETERS

- $V_{OL}/V_{OH}/V_{IL}/V_{IH}$
- $I_{OL}/I_{OH}/I_{IL}/I_{IH}$
- V_{DD}/V_{CC}
- I_{DD}/I_{CC}

Functional / AC Testing

- Functional Test will test the functionality / logic for the best / worst conditions.
- AC Test will check the Timings (Frequency, Pulse widths, setup and hold times and delays etc)
- Pass/fail limits for each parameter

Some AC PARAMETERS

- Propagation Delay
- Rise/Fall time
- Frequency
- Duty Cycle
- Pulse Width
- Setup/Hold time

Device Specifications

- Device specification must be clearly understood before starting to write the test programs.

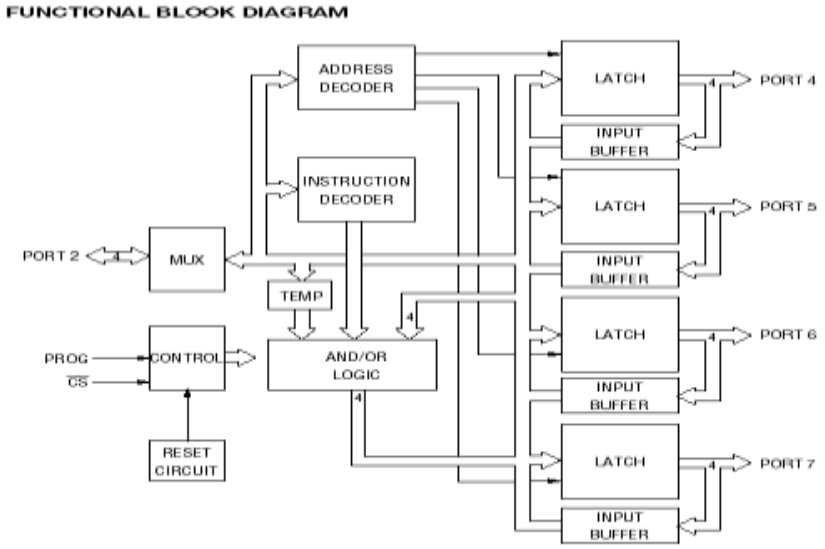
- Various specifications are listed below :
  a) Functional Description
  b) DC Specification
  c) AC Specification

Functional Specification

- Usually Device Specification begins with functional description and block diagram.

- Functional Logic will be available as truth table if the logic is simple. For complex devices logic function will be described in details.

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H



Revise

DC Specifications

- DC Section defines the following operating parameters of the device

  a) Maximum Ratings
  b) Operating Range
  c) DC Characteristics
  d) Capacitance

DC Specifications

DC PARAMETERS

V_{DD}	The supply voltage to a **CMOS** device
V_{CC}	The supply voltage to a **TTL** device
I_{DD}	The current drawn from the supply for a **CMOS** device
I_{CC}	The current drawn from the supply for a **TTL** device

DC Specifications

V_{OH}	The worst case (min) voltage at the **output** that drives a **logical 1**
V_{OL}	The worst case (max) voltage at the **output** that drives a **logical 0**
I_{OH}	The **maximum** current the **output** can **source** when driving a **logic 1**
I_{OL}	The **maximum** current the **output** can **sink** when driving a **logic 0**

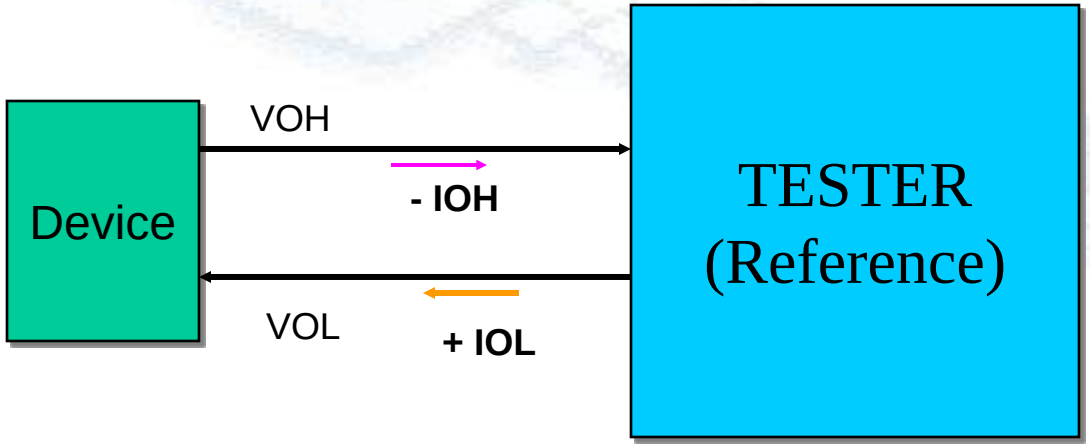
DC Specifications

V_{IH}	The worst case (min) voltage at the **input** that is recognized as **logical 1**
V_{IL}	The worst case (max) voltage at the **input** that is recognized as **logical 0**
I_{IH}	The worst case (max) current the **input** pin can **sink** to maintain **logic 1** voltage at output of the device it is connected to
I_{IL}	The worst case (max) current the **input** pin can **source** to maintain **logic 0** voltage at output of the device it is connected to

DC Specifications

Conventions:

- When current flows **OUT** of a device, the device is said to **SOURCE** current.
- Conversely, when current flows **INTO** a device, the device is said to **SINK** current.



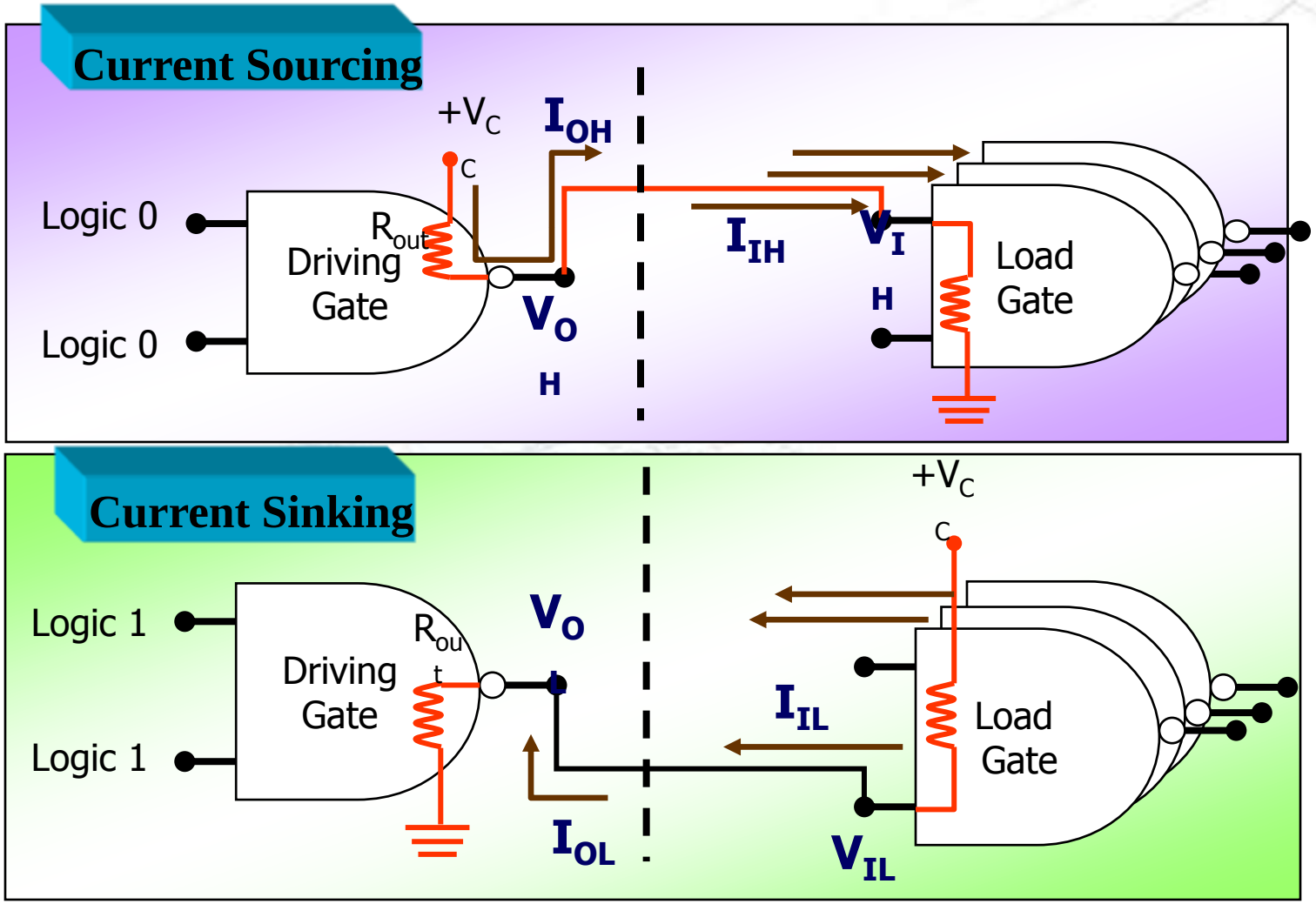
Typical VOL / VOH

- VOL is output low voltage
- VOH is output high voltage
- TTL VOL = 0.4V
- TTL VOH = 2.4V
- CMOS VOL=0.1V (GND + 0.1) @ No load
- CMOS VOH=4.9V (VDD – 0.1) @ No load

IOL / IOH

- IOL is output sink current
- IOH is output source current
- Output pin will source the current when it drive logic high.
- Output pin will sink the current when it drive logic low.

DC (Current) Parameters



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VIL / VIH

- VIL is input low voltage
- VIH is input high voltage
- TTL VIL = 0.8V
- TTL VIH = 2.0V
- CMOS VIL=1.5V (VDD x 0.3)
- CMOS VIH=3.5V (VDD x 0.7)

Power Supply Current (IDD)

- IDD is the measure of total current that flow`s into the power supply pin.
- The IDD static current test ensures that the DUT will not consume more current than the value stated in the device specifications
- Generally, two types of current checks are performed:
  - IDD Static Current check: DUT is inactive
  - IDD Dynamic Current check: DUT is active

Tristate Leakage Current (IOZ)

- IOZ is output high impedance leakage current.
- IOZL is the measure of output impedance leakage current from the output pin to VDD when the output pin is in tri state(high impedance state).
- IOZH is the measure of output impedance leakage current from the output pin to GND when the output pin is in tri state.

AC Specifications

Propagation Delay

Delay from the time a signal is applied to the time when the output makes its change

Rise Time

The time required for an edge to go from (typically) 10% to 90% of its high limit voltage value

Fall Time

The time required for an edge to go from (typically) 90% to 10% of its low limit voltage value

AC Specifications

Duty Cycle

The ratio of the positive pulse width to the period (positive duty cycle)

Pulse Width

Positive pulse width is the period of time from the midpoint of a rising edge to the midpoint of the immediate falling edge.
Negative pulse width is the period of time from the midpoint of a falling edge to the midpoint of the immediate rising edge.

Frequency

To measure the maximum operating frequency of the device.
(Period = 1/Frequency)

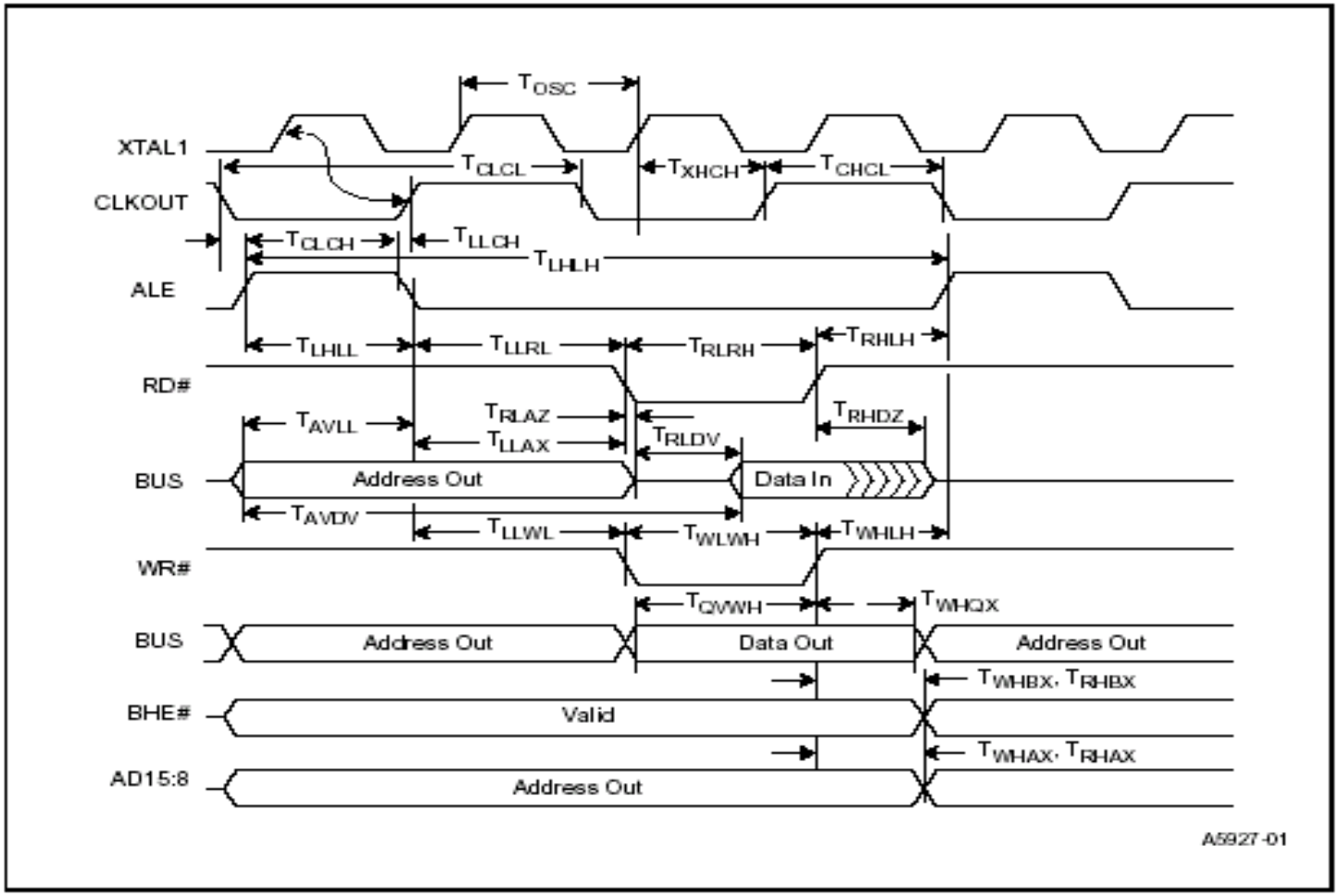
AC Specifications

- AC Section contains the timing diagrams and individual parameter values of the device.
- It defines the type of AC load circuit to be used while testing the output timing parameters
- Further pages contain the sample datasheet of a device.

AC Specifications

87C196CA 18 MHz Microcontroller — Timing diagram

Figure 5. System Bus Timing



Sample Specifications

PARAMETER	TEST CONDITIONS‡			SN5400			SN7400			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −12 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = 0.8 V,	I_{OH} = −0.4 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.4 V				40			40	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				−1.6			−1.6	mA
I_{OS}¶	V_{CC} = MAX			−20		−55	−18		−55	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			4	8		4	8	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			12	22		12	22	mA

Revised 8/8/2007

Sample Specifications

recommended operating conditions (see Note 3)

		SN5400			SN7400			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{OH}	High-level input voltage	2			2			V
V_{OL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN5400 SN7400			UNIT
				MIN	TYP	MAX	
t_{PLH}	A or B	Y	R_L = 400 Ω, C_L = 15 pF		11	22	ns
t_{PHL}					7	15	

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Self-Assess Questions

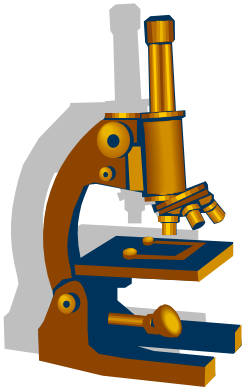
1. Which of these below should be included in a Testplan?

   Hardware Requirement, List of Test to performed, Timeline/Schedule

2. What is the difference between Hard Binning and Soft Binning?

3. Name at least 3 common categories of test performed on a semiconductor device.

DC PARAMETERS TEST



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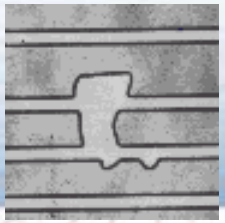
Continuity/Open-Short Test

The Continuity test checks for :

1. Device problem - Open/Shorted device pins. The cause for opens or shorts can be due to error in fabrication of die or problems in the physical packaging of the die like missing bond wires, shorted pins, pin damaged by static electricity etc

2. Tester system problem - poor interfacing between DUT and testing equipment. Poor electrical contact between tester (ie socket) or bad wafer probe card etc

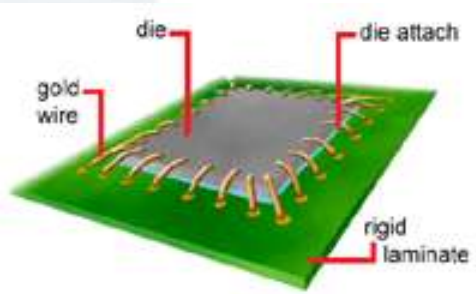
What is Open/Short Test ?



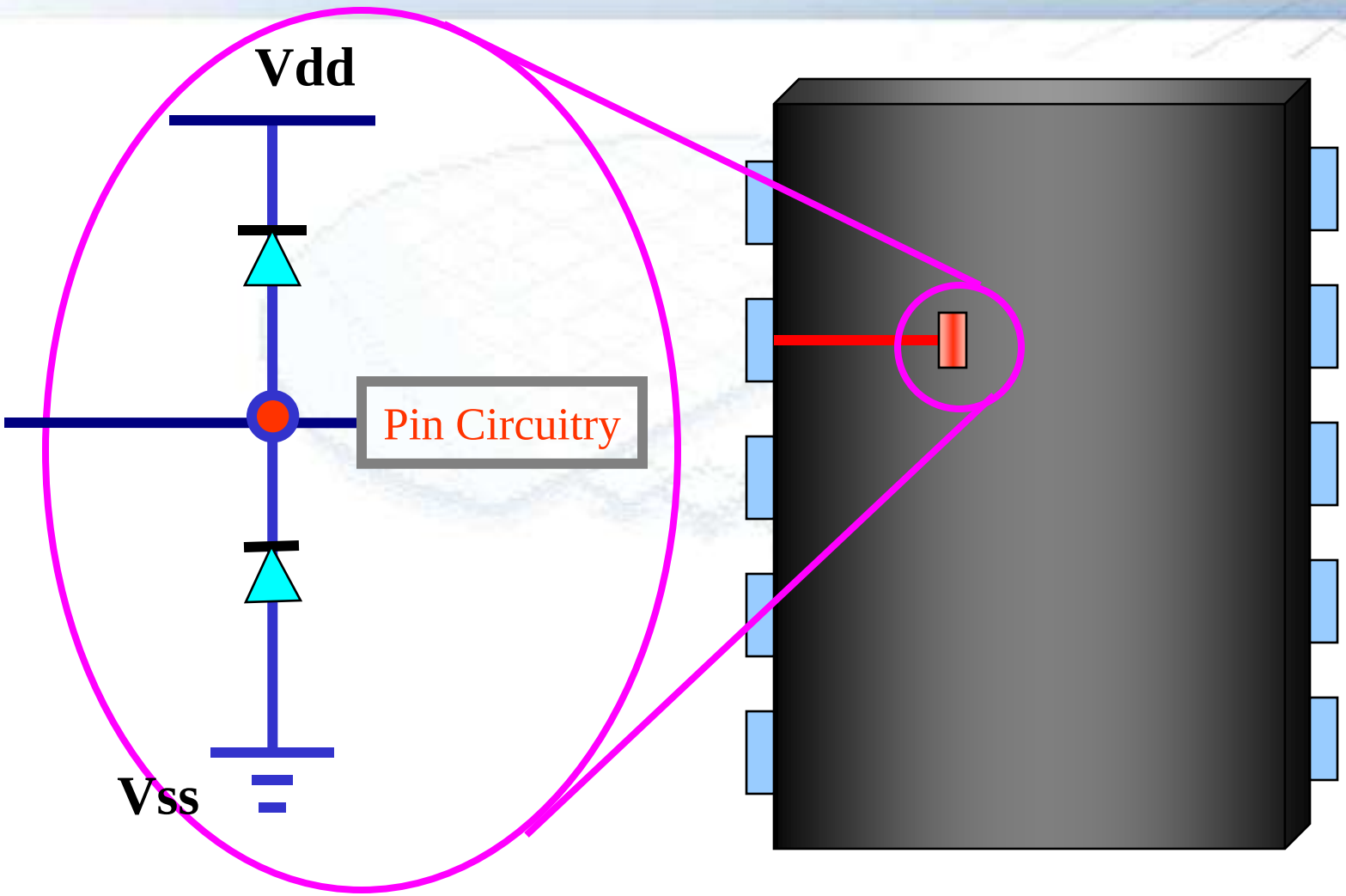
- This is typically the first test performed (at package and wafer).
- Open test can identify the missing bond wire problems.
- Short test can identity the illegal short between pins.
- This is very simple test and can be done very faster which reduce the average test time of bad devices
- Another name for open/short test is continuity test.

Types of Open/Short Test

- DC Test method/ Serial Static method
- Functional Test method



MODEL OF 1 DEVICE PIN



Test Concept

- PMU will be used in Force Current Measure voltage mode to perform the Open / Short test.
- This test is done by making use of the protection diodes on the device pins, specifically by forcing a positive or negative current into the pin and measuring the resultant voltage across the diodes, it can be determined if the pin under test is shorted or open.
- This is done repeatedly as each pin is individually tested.

Test Concept

Input Stimulus:-

+Current or –Current

Expected Response:-

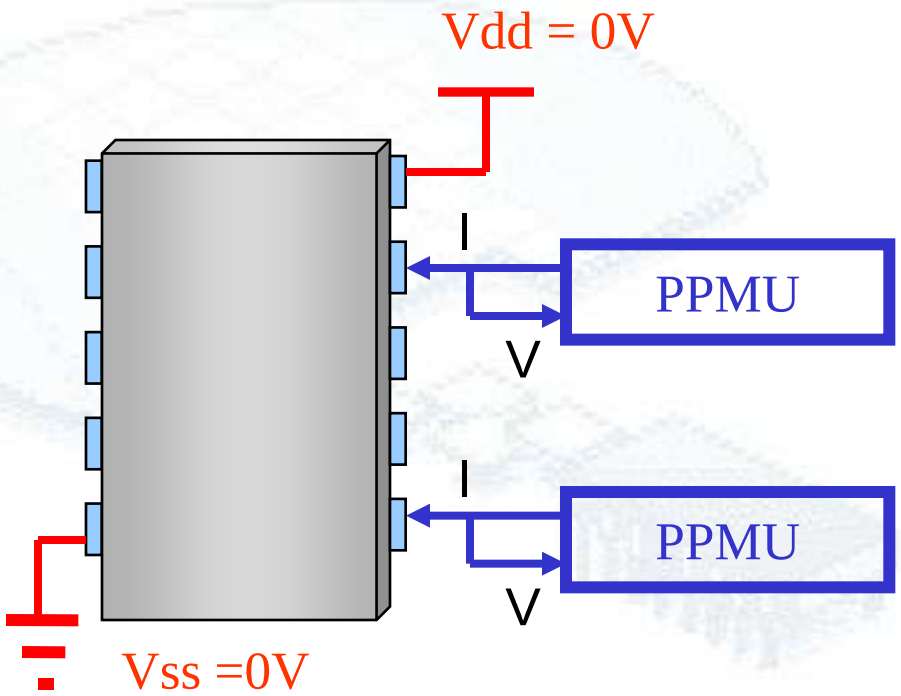
Voltage level dropped across protection diode

Test Condition(s):-

Power supply voltage set to 0V

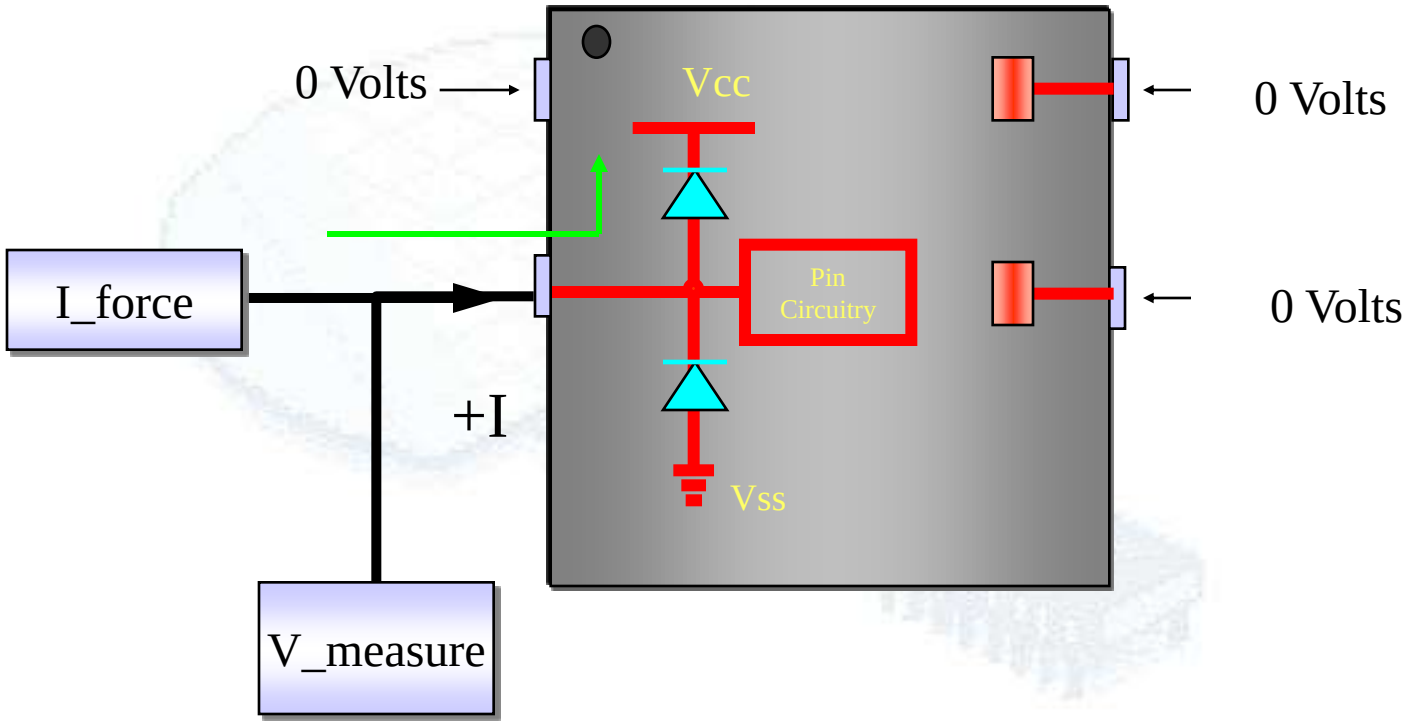
Continuity Test Setup

Continuity Test



Using Pin PMU in force current and measure voltage mode

Test mode: FORCE I, MEASURE V
One pin at a time



Fail open : V_measure > 1.5 V
Fail Shorts : V_measure < 0.2 V

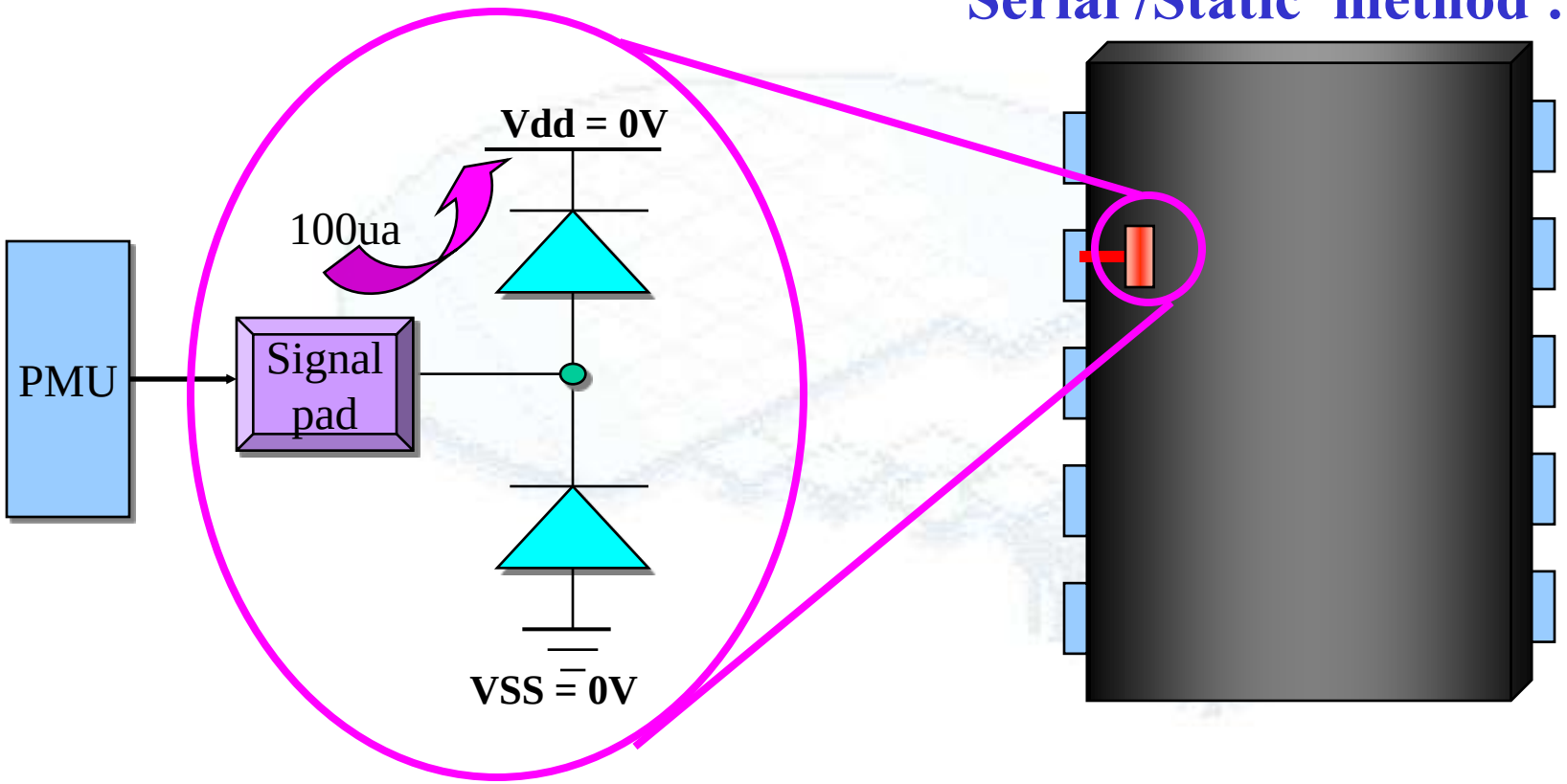
DC Test method cont…

How to program?

1. Drive 0.0V at all power pins (VDD, VSS etc…) and input/output pins except the pin under test of the DUT.
2. Force current can be 100µA to 500 µA. Let us consider we are driving 0.1mA for pin under test of the DUT which will forward bias the VDD diode.
3. Clamp voltage can be set as 3.0V
4. If the measured voltage at pin under test is around +0.7V, it passes for Open/Short Test.
5. If the measured voltage is 0.0V, pin has illegal Short
6. If the measured voltage more than 1.5V, pin is Open.
7. Similarly, all other pins of DUT will be tested.

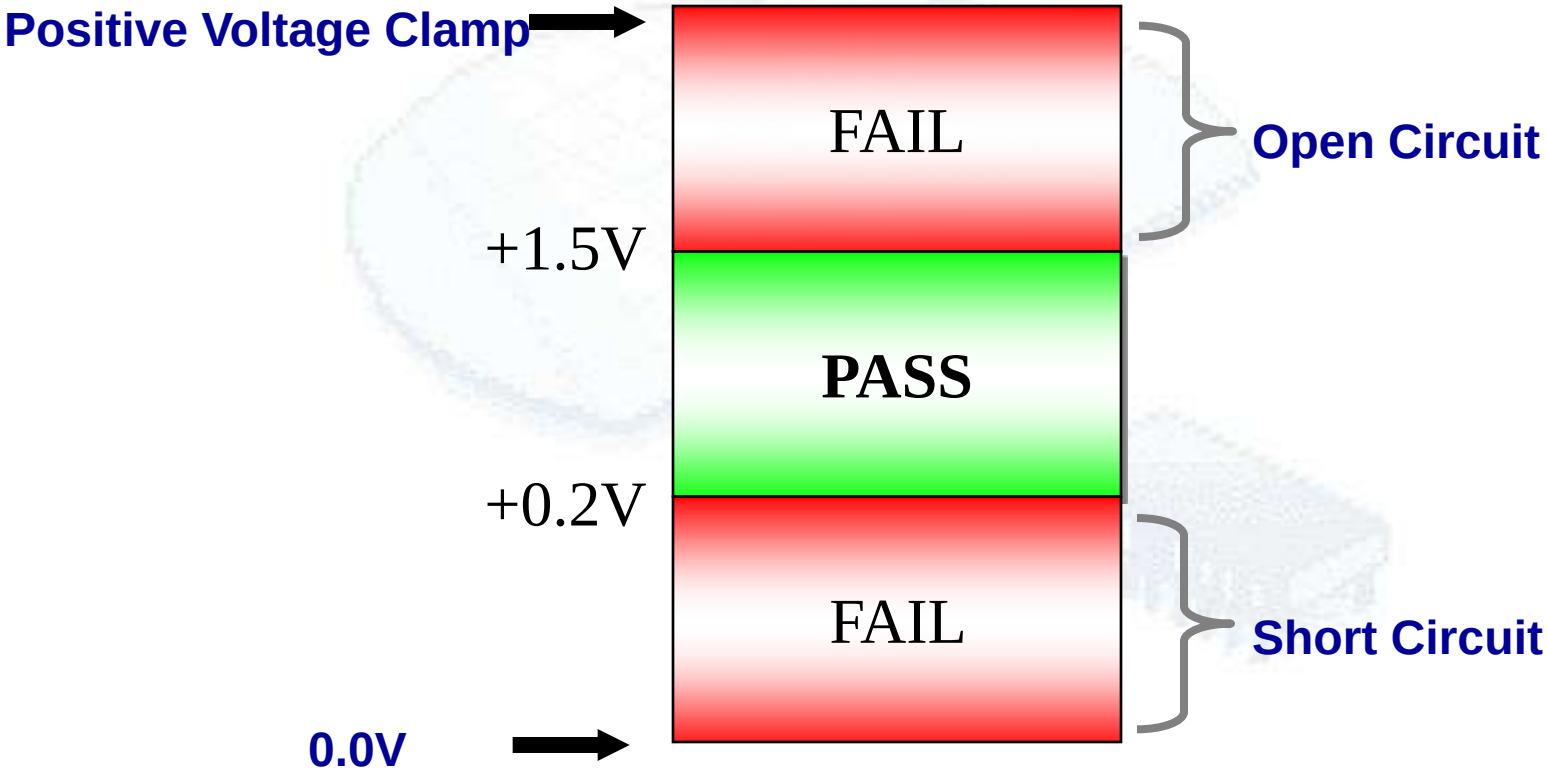
Continuity Test

Serial /Static method …



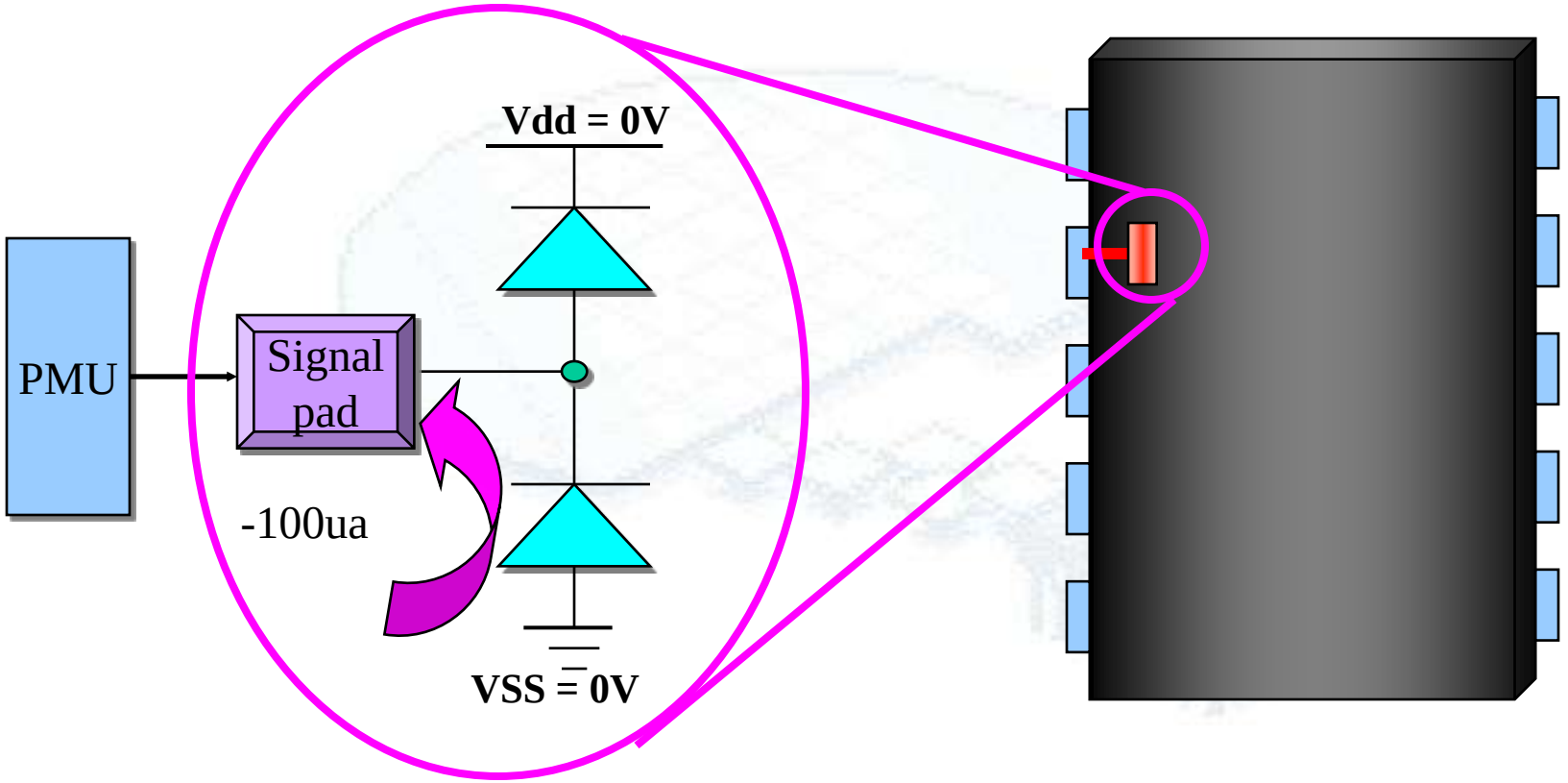
VDD Diode test

VDD Diode Test Results



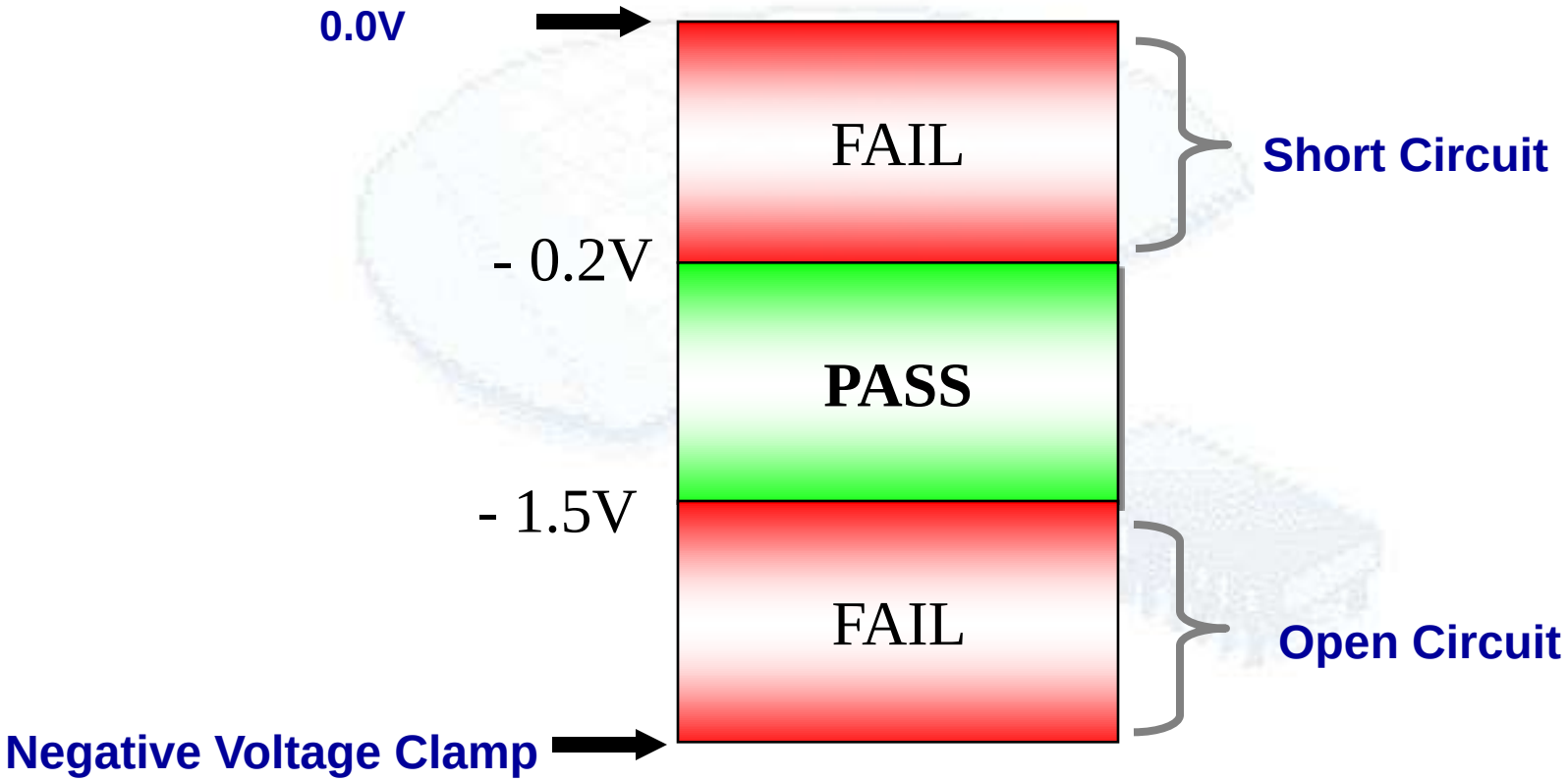
Continuity Test

Serial /Static method …



GND Diode test

GND Diode Test



Functional Continuity Test Method

- Active Load / Functional Comparator will be used to perform the Open / Short test.
- Negative or Positive current will forward bias the VSS or VDD protection diode and received digital output of each pin will be compared as explained in following page.

Functional Test Method (cont…)

1. Drive 0.0V at all power pins (VDD, VSS etc…) and input/output pins except the pin under test of DUT.
2. Set VOH = 1.5V & VOL = 0.2V
3. Isrc = 0.1 mA & Vref = 3.0V
4. If the received vector at pin under test is Z (Hi-Impedance), it passes for Open/Short Test.
5. If the comparator sense a output low “L” (less than 0.2 V), pin has Short
6. If the comparator sense a output high “ H” (more than 1.5V), pin is Open.
7. Similarly, all other pins of DUT will be tested with the pattern.

DC Continuity Test (sample datalog)

Fail open

Number	Site	Result	Test Name	Pin	Channel	Low limit	Measured	High limit	Force
200	0	FAIL	cont_p2	p23	7	-1.5000V	-8.630 V	-200.0000 mV	-100.0000 uA
201	0	PASS	cont_p2	p22	31	- 1.5000V	-785.3 mV	-200.0000 mV	-100.0000 uA
202	0	PASS	cont_p2	p21	23	- 1.5000V	-953.0 mV	-200.0000 mV	-100.0000 uA
203	0	PASS	cont_p2	p20	48	- 1.5000V	-877.4 V	-200.0000 mV	-100.0000 uA
204	0	FAIL	cont_ctr	cs	4	- 1.5000V	-0.0004 mV	-200.0000 mV	-100.0000 uA
205	0	PASS	cont_ctr	prg	30	- 1.5000V	-943.96 mV	-200.0000 mV	-100.0000 uA

Fail shorts

In the above example pin ‘cs’ is failed due to Continuity short & ‘P23’ has failed due to Continuity open

Revised 8/8/2007

Comparison

	DC Test	Functional Test
1	Slower	Faster
2	Can write the detailed data log for further failure analysis.	Can’t get detailed log.

Generally Functional continuity test can be performed first and “if” functional continuity test fails then immediately the DC continuity Test can be conducted.

WHY Continuity test fail?

COMMON DEBUGGING ACTIONS IF DEVICES FAIL CONTINIUITY IN PRODUCTION

Retest the device!

The protective diodes are sometimes faulty but such cases are RARE.

Typically, failure of continuity test results are system not receiving the part correctly or probe faults.

Hence, always set a limit for prober/handler maximum consecutive failure number.

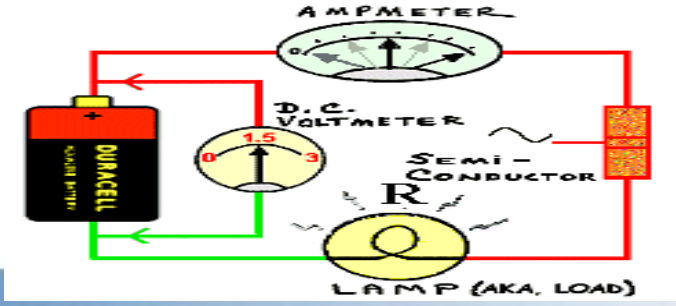
If the probes or socket is damaged, halt further testing and contact the maintenance personnel.

DC Parameters Test - Overview

- Power Supply Current (IDD) Test and Test Method
- Static IDD ,Dynamic IDD, IDDQ Test method
- IIL/IIH and Test Methods
- IOZL/IOZH and Test Methods
- IOS and Test Methods
- VOL/IOL and Test Methods
- VOH/IOH and Test Methods
- Fanouts

What is DC Test ?

- DC parameters are tested by forcing current and measuring voltage or forcing voltage and measuring current.
- In both ways, only resistivity of silicon is being measured.
- Device conductive/resistive specs may differ as fully-conducting, semi-conducting or non-conducting.
- During DC test voltage or current is measured and the pass fail results are based upon the measured value.



Power Supply Current Test

- Purpose / Why test
- Impact
- Test concepts
- Terms
- Test methods
- IDD Gross Test method
- IDD Static /Dynamic Test method
- IDDQ Test method

Why test Power Supply Current

- Measures how much power supply current the DUT consumes when it is powered up
- The main reason is to guarantee limited power consumption in the customer's end application. Supply current is an important electrical parameter for the customer who needs to design a system that consumes as little power as possible.
- The Power Supply Current test checks for catastrophic defects in the device. The cause for catastrophic defects can be due to under-etching and/or photo-mask misalignment during fabrication process.
- Typically, Power Supply Current Test is performed after Continuity and Leakage Tests, prior to Functional Testing

Test Concept

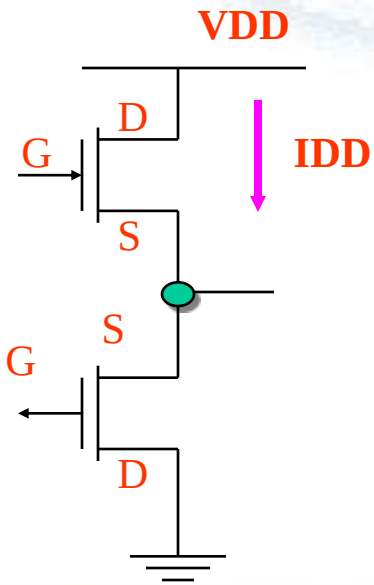
- This test is done by measuring the current flowing from each voltage source connected to the DUT.
- The power supply is simply set to the desired voltage and the current from its output is measured.
- Gross IDD is a quick check for IDD, before continuing with further tests.
- Generally, two types of current checks are performed:
  1. IDD Static Current check: DUT is inactive
  2. IDD Dynamic Current check: DUT is active
- The above is done repeatedly for each power supply pin as each pin is individually tested.

TERMS

V_{DD}	The supply voltage to a **CMOS** device
V_{CC}	The supply voltage to a **TTL** device
I_{DD}	The current drawn from the supply for a **CMOS** device
I_{CC}	The current drawn from the supply for a **TTL** device

IDD Gross Current

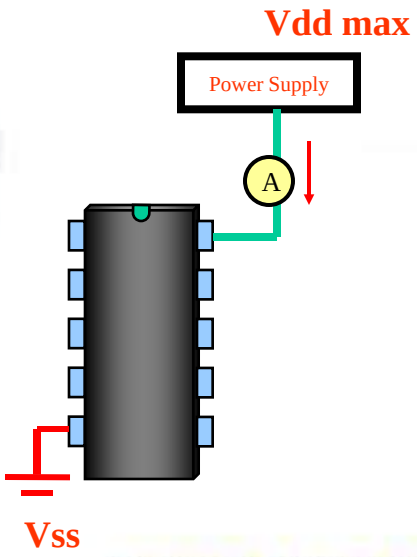
- For the CMOS devices the current flow between drain to drain is represented as IDD.
- For the TTL devices, it is represented as ICC (collector to collector current).
- Gross indicates that the measurement made in relaxed conditions which is defined in Specification.



Why Gross IDD Test ?

- Used to measure the impedance between VDD and GND of the DUT.
- To quickly determine whether it is reasonable to continue the test.
- Mostly, this test will be performed after Continuity test.
- This is power on Test.
- Test system may get affected if DUT draws excessive current.

  If this test fails, test will be aborted and DUT will be rejected.



Gross IDD - Test Method

- Since we are performing this before functional test, test limits should be relaxed
- Output should not be connected with load.
- Test limit should be 2 to 3 times greater than the device specification.
- If the IDD is not specified in the specification, number of devices should be tested and average current should be set as test limit.
- Use DPS or System PMU for this test.

Gross IDD - Test Method cont..

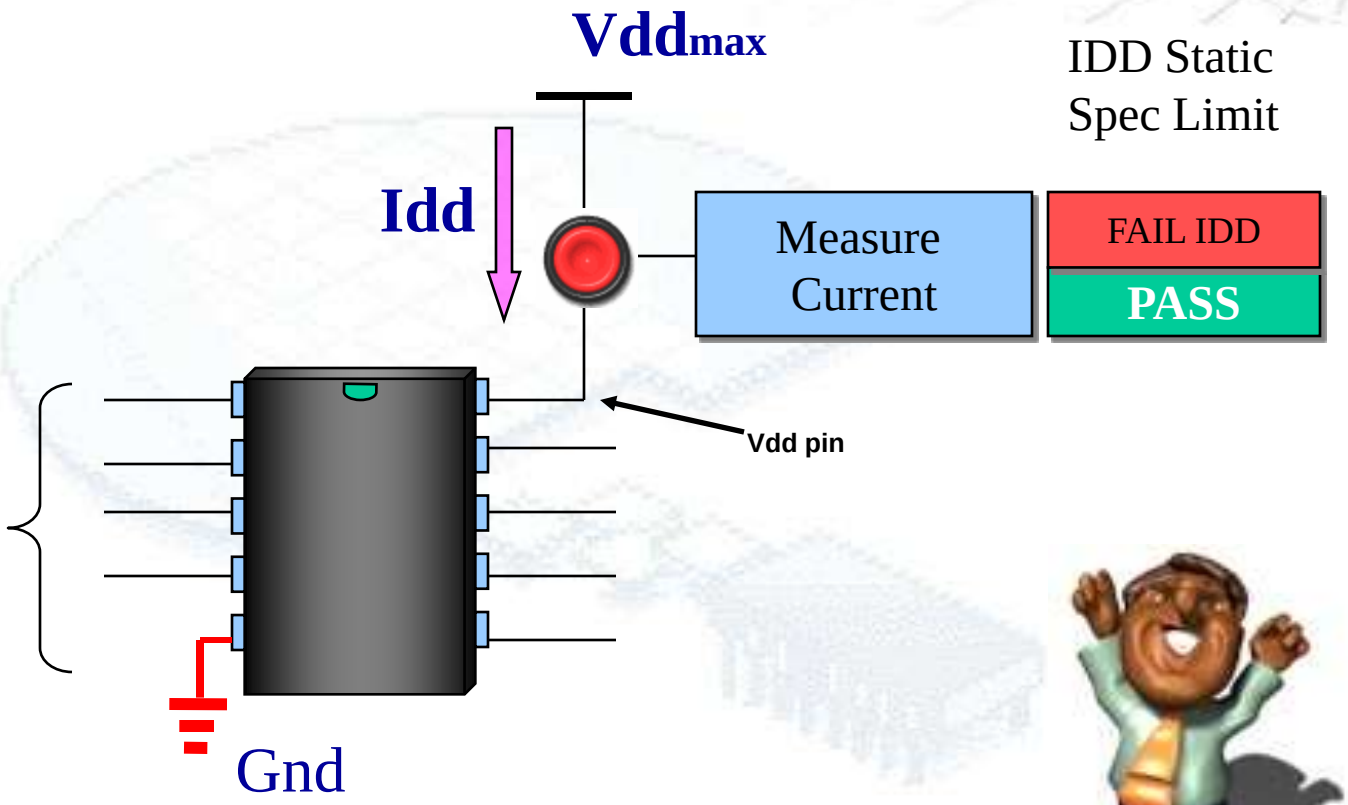
Gross IDD for troubleshooting

- Used to measure the impedance between VDD and GND of the DUT.
- After developing the test program, if we come across with Gross IDD failure, takeout the device from socket and test it to measure 0ma current.
- If still fails, we can conclude something else is consuming the current from test system. Load board can also be removed to confirm the problem.

Static IDD Current & Why ?

- Static indicates that the measurement is made when DUT is not active.
- To ensure that the DUT will not consume more current than the available value in the Specification.
- This is important for battery operated devices.
- To identify the processing problems with CMOS devices.

Static IDD - Test Method



- Resultant IDD Static current is measured and compared against the test limits .

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Static IDD - Test Method

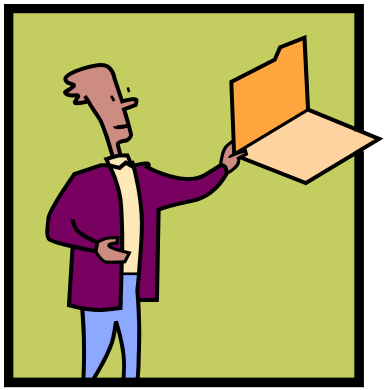
- DUT should be exactly preconditioned for the state which consumes least IDD current.
- If the IDD current is small, additional delay time should be given.
- External by-pass capacitors should be disconnected using relays to avoid low IDD current measurement problems.
- The DUT is held in a static condition and the amount of current flowing into the supply pin is measured, compared to the IDD static device specifications.

Dynamic IDD Current & Why ?

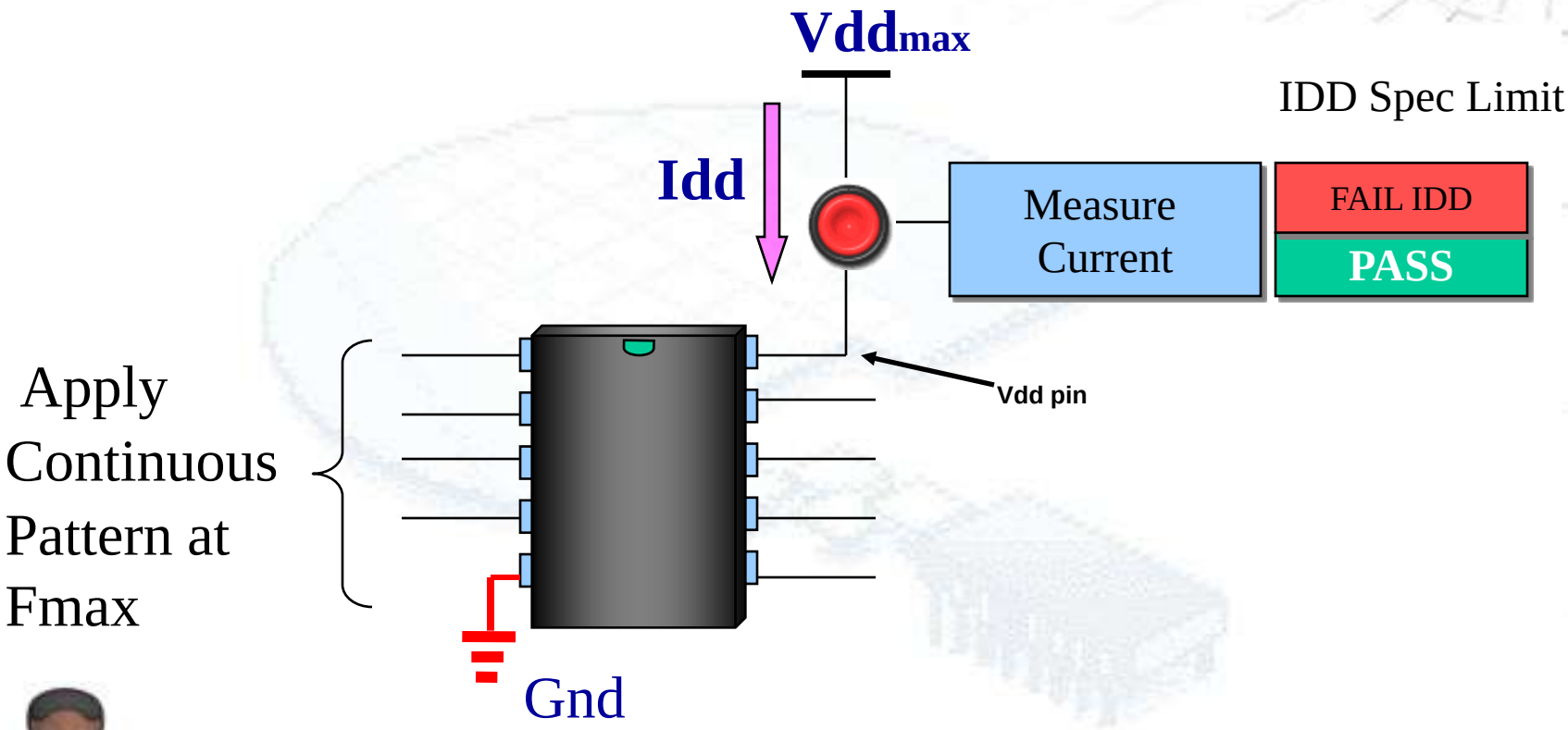
- Dynamic IDD is the operating IDD of the device.
- The IDD dynamic current test insures that the DUT will not consume more current than the value stated in the device specifications while the DUT is actively performing its functions.
- This test measures total current flow into the power supply pin.
- Performed by executing a test vector pattern, normally at the maximum operating frequency of the DUT.
- The resultant current measurement is compared to the IDD dynamic device specifications.

Dynamic IDD - Test Method

- Dynamic IDD measured when the DUT is driven by continuous pattern at maximum operating frequency.
- VIL, VIH, VDD, Fmax are influencing the test results.
- Dynamic IDD should produce consistent results when the test is repeated.



Dynamic IDD - Test Method



- Resultant IDD dynamic current is measured and compared against the test limits .

Revised 8/8/2007

IDDQ Current & Why ?

IDDQ is quiescent current

- A technique for finding shorts in CMOS devices that tests for quiescent power supply current (Iddq).
- IDDQ testing has become a standard test technique used to reduce PPM levels and detect reliability defects in silicon used for high reliability applications.
- IDDQ (Quiescent IDD) testing is a useful to find long-term reliability failures, due to partially functioning logic that did not fail during standard testing.

IDDQ Test

- This test performs static IDD measurements at unique points within a functional vector set . (Typically 5 to 10 measurements)

- The test vector sequence for this this test is to toggle on and off as many transistors as possible and measure at the different vector sequence stopping points.

IDDQ Test

- Set the VDD to VDDmax.
- Start the IDDQ test vector.
- Stop at the test point and hold the device at the know state.
- Measure the current flow between the VDD & VSS.
- Typical limits will be in micro_amps for a complex CMOS device.

.

Advantages of IDDQ

Diagnosing defects using IDDQ offers several advantages because:

- IDDQ is a cost-effective test method indispensable to identify some defects which are not detectable by the conventional functional tests.

- IDDQ enhances quality, shortens time-to-market and provides an efficient SPMC (Statistical Process Monitor and Control) for yield enhancement.

The types of potential problems detected by IDDQ include:

- Process flaws: bridging, deformed traces, mask problems, incomplete etching, logically redundant defects.

- Design flaws: Floating gates, logic contention, mask generation errors.

IDD Test

- IDD tests are often performed with the device in several different states
  - Different power up states
  - Power off (or “sleep”) state
  - Some devices have different operating modes to power down different sections
  - These provide for ease of identification of sections that do not properly shutdown

- Device may have several different power pins which go to separate tester supplies
  - IDD value = Sum of DUT(Idd1) + DUT(Idd2) + ...

Leakage Test

Topics to cover:

- Purpose / Why test
- Impact
- Test concepts
- IIl/IIH and Test Methods
- Serial/Parallel/Ganged Test Methods
- IOZL/IOZH and Test Methods
- IOS and Test Methods

Leakage Test: Purpose/Why

The Leakage test checks for :

Leakage in input current. It ensures that the input current meets the design requirements i.e. the input pins does not sink/source more than the current specified by the specifications.

Too high leakage current for certain pins could result from variations in fabrication process or the pin could be damaged from static electricity.

The cause of leakage current could be due to presence of an alternative lower resistive path

Why Leakage Test ?

- Measures the resistance from input pin to VDD/GND.
- Insures that input will not draw more than the specified IIL/IIH current when it is forced for low or high.
- Identify processing problems in CMOS devices.
- Typically this is one of the earlier tests performed, usually after Continuity

Test Concepts

Leakage is measured by simply forcing a DC voltage on the input pin of the device under test and measuring the small current flowing into or out of the pin.

Leakage is typically measured twice:

- measured once with an input voltage voltage near the positive power supply voltage, and
- measured again with the input near ground (or negative supply)

These two currents are referred to as I_{IH} (input current, logic high) and I_{IL} (input current, logic low) respectively.

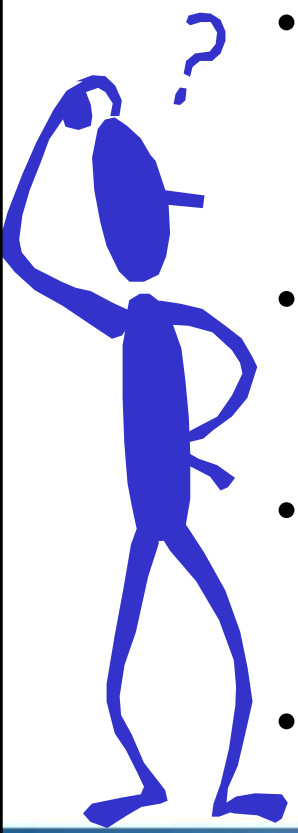
Test Concept

The approach to testing for Leakage Current is straightforward.

- The device specifications states the limits for I_{IH} and I_{IL} for the device when certain voltage level is forced on the input pins.
- We take the worst case limit as the limit for our test program.
- VDDmax is the worst case test condition for these test.
- Before going into the details of the test, a brief section on the likely causes of leakage current is covered.

What happens if a pin is leaky ?

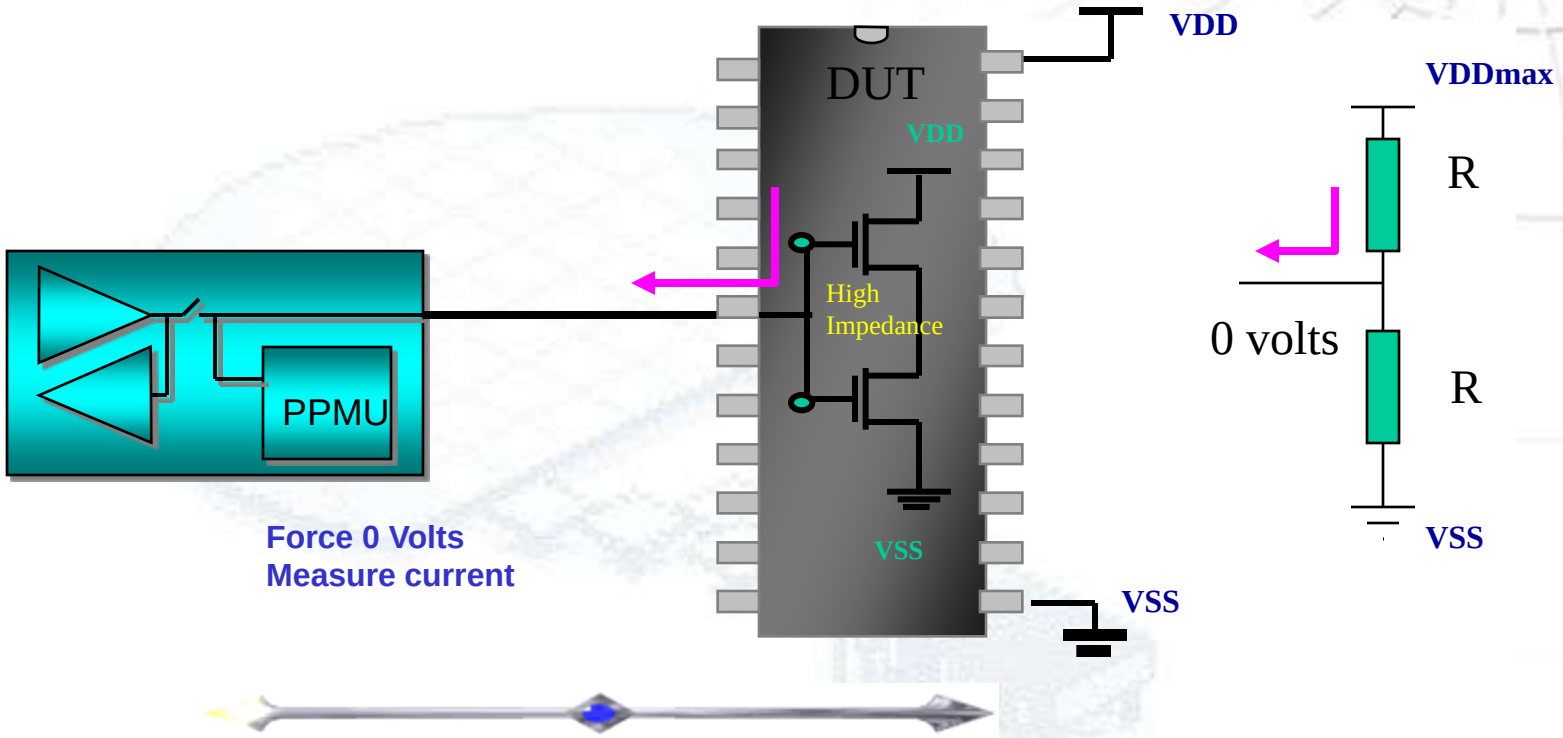
- Leakage is likely due to the presence of a lower resistive path
- Overall current flow through the test pin INCREASES due to the DECREASE in overall (input) resistance of the test pin
- Leakage Testing tests for leakage of current from a test pin to adjacent pins
- Eventually, further changes will violate the maximum I_{IL}/I_{IH} limit
- The result is a failure in the Leakage Test



IIL Test – Serial Method

- All input pins are preconditioned for logic high state except the pin under test.
- PMU is connected to pin under test and then forces this input low and the resultant current is measured and compared with the specification limits.
- The above is repeated for each input pin applicable

IIL Test – Serial Method

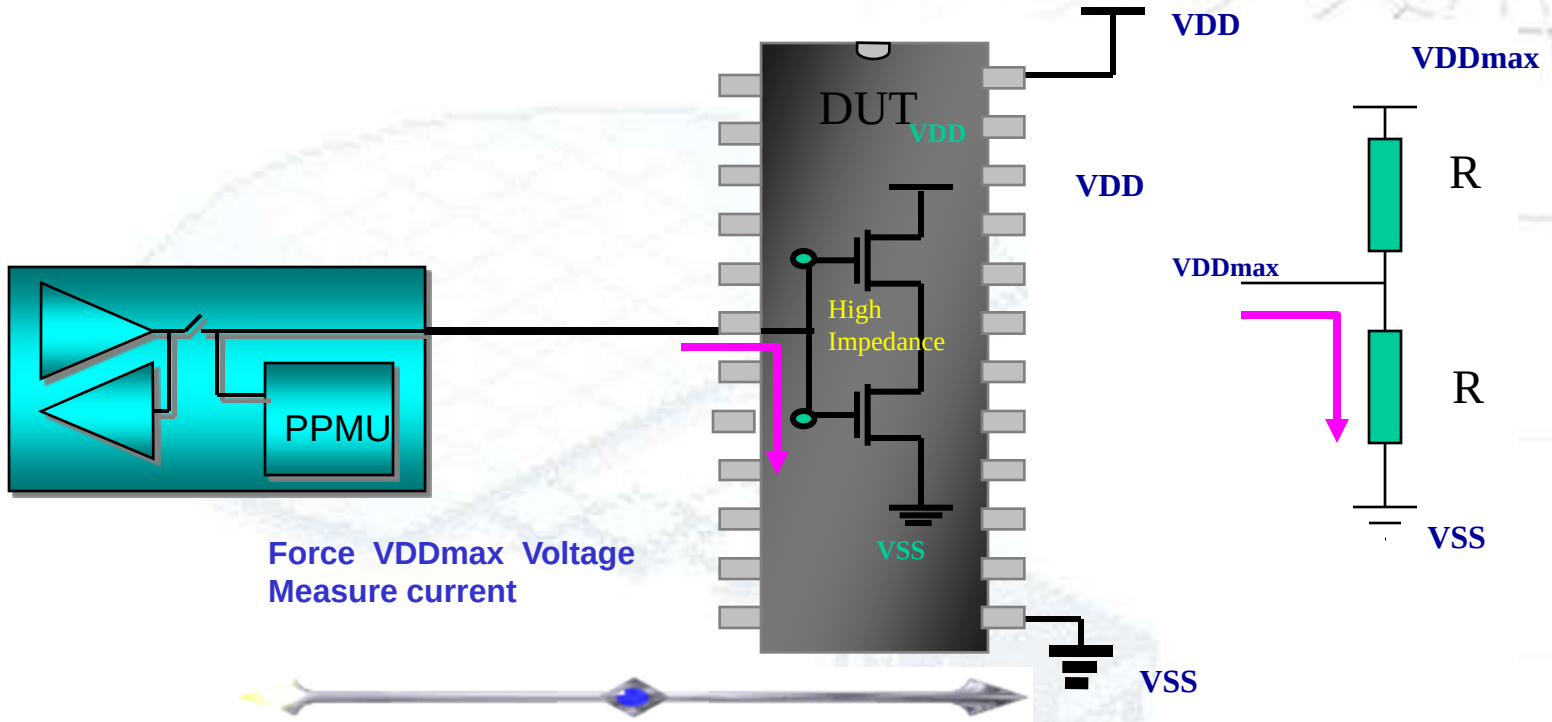


- Performed by forcing a Zero voltage on the particular pin under test
- Measure the resulting current into the pin
- If “leaky,” amount of current into or out of the pin under test will be > Spec Value

IIH Test – Serial Method

- All the input pins are set to zero volts except the pin under test.
- PMU is connected to pin under test and forced high. The resultant current is measured and compared with the specification limits.

Test Method for IIH

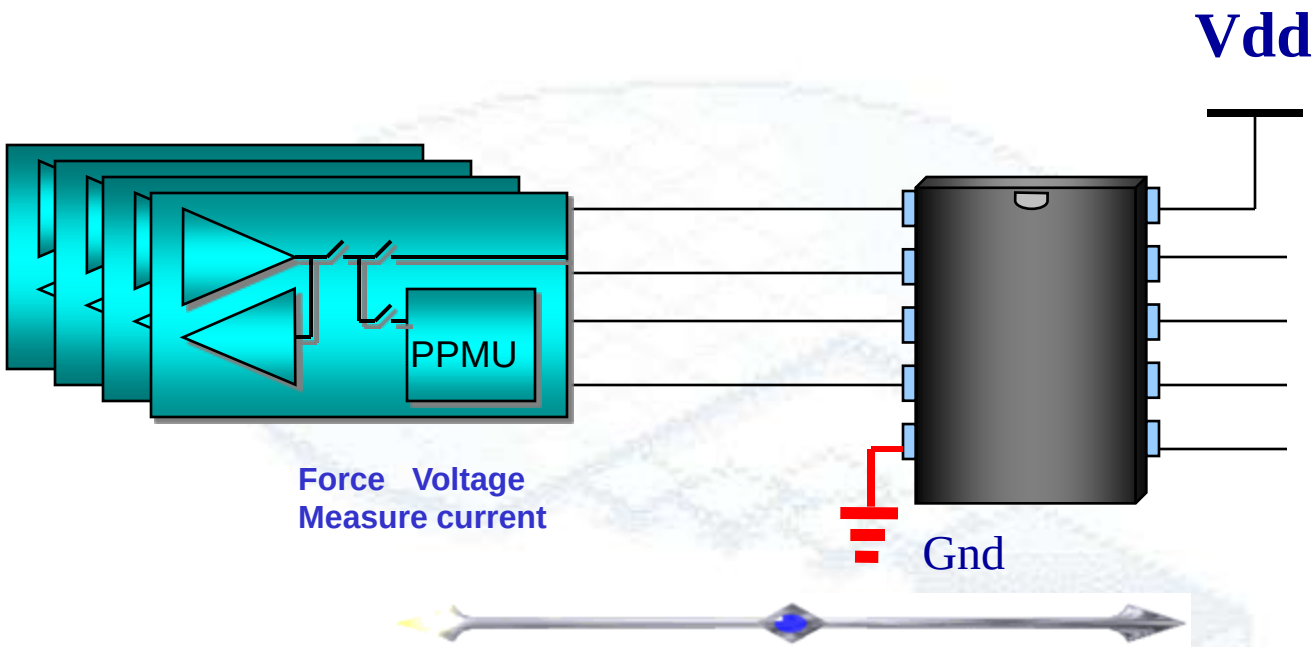


- Performed by forcing the Vddmax voltage to the particular pin under test
- Measure the resulting current into the pin
- If “leaky,” amount of current into or out of the pin under test will be > Spec Value

IIL/IIH Parallel Test Method

- Some Test Systems are having per Pin PMU.
- Parallel measurement means all inputs will be driven low simultaneously and measurement will be made for IIL test.
- Similarly, all pins will be driven high and measurement will be made for IIH test.
- Parallel test method can not identify the leakage between input pins as we are testing all pins simultaneously.

IIL/IIH Parallel Test Method



- Test is performed two time by forcing Vddmax(IIH) and Vss(IIL) using PMU
- Program a delay of 1 to 5 ms wait time .
- Resultant current is measured and compared against the test limits .

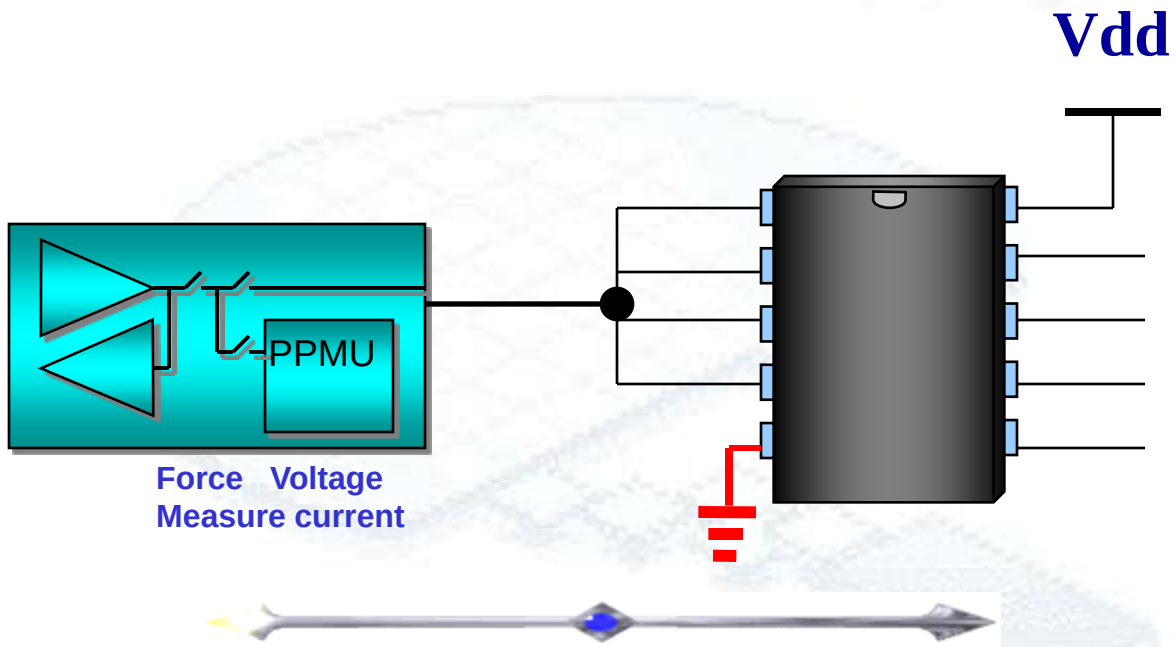
Advantages / Disadvantages Parallel Test Method

- Advantage of this method is the test can be performed faster and all the device pins are tested for its leakage.
- Disadvantage is pin to pin leakage cannot be detected as all the pins are at same voltage level.
- This method requires the system to have per pin PMU hardware.

IIL/IIH Ganged Test Method

- Ganged Test method is nothing but connecting a single PMU to all inputs at one time and measuring total current flow.
- It can be used mainly for high impedance CMOS inputs not for resistive inputs.
- Ganged testing will not work if different pin consumes different current.

IIL/IIH Ganged Test Method



- Force Vddmax (to test for IIH) using PMU
- Program delay time of 1 to 5 ms.
- Measure resultant (total) current and compare against the test limits
- Repeat the above with by forcing Vss(IIL)

Advantages / Disadvantages Ganged Test Method

- Advantage of this method is the test can be performed faster and it doesn`t require per pin PMU.
- Disadvantage is that individual pin leakage current cannot be measured.
- Both ganged and serial method can be used together. If ganged-test fails, serial test method will then be executed, to find the exact failing pin for leakage.

Leakage Test (Sample Datalog)

Number	Site	Result	Test Name	Pin	Channel	Low limit	Measured	High limit	Force
150	0	**FAIL**	ppmu_loleak_p2	p23	7	-10.0000 uA	-18.2912 uA	10.0000 uA	0.0000 V
151	0	PASS	ppmu_loleak_p2	p22	31	-10.0000 uA	875.1700 pA	10.0000 uA	0.0000 V
152	0	PASS	ppmu_loleak_p2	p21	23	-10.0000 uA	-5.0839 nA	10.0000 uA	0.0000 V
153	0	PASS	ppmu_loleak_p2	p20	48	-10.0000 uA	-5.1774 nA	10.0000 uA	0.0000 V
154	0	PASS	ppmu_loleak_ctr	cs	4	-10.0000 uA	1.6501 nA	10.0000 uA	0.0000 V
155	0	PASS	ppmu_loleak_ctr	prg	30	-10.0000 uA	-1.2792 nA	10.0000 uA	0.0000 V
156	0	**FAIL**	ppmu_hileak_p2	p23	7	-10.0000 uA	32.7916 uA	[illegible]	5.5000 V
157	0	PASS	ppmu_hileak_p2	p22	31	-10.0000 uA	10.9652 nA	[illegible]	5.5000 V
158	0	**FAIL**	ppmu_hileak_p2	p21	23	-10.0000 uA	12.4392 uA	[illegible]	5.5000 V
159	0	PASS	ppmu_hileak_p2	p20	48	-10.0000 uA	2.3655 nA	[illegible]	5.5000 V
160	0	PASS	ppmu_hileak_ctr	cs	4	-10.0000 uA	26.8562 nA	10.0000 uA	5.5000 V
161	0	PASS	ppmu_hileak_ctr	prg	30	-10.0000 uA	18.8714 nA	10.0000 uA	5.5000 V

Fail IIL

Fail IIH

Fail IIH

In the above example pin P23 is failed for both IIH and IIL & P21 has failed for IIH current

IOZL/IOZH

- IOZL is the current from high impedance output when output is forced for logic Low.
- IOZH is the current from high impedance output when output is forced for logic High.

What is a Tristate ?

- Tristate is often called as floating or Z state. When an output is tri-stated it looks like high impedance to another device.

- Requires an additional control input, typically called an Enable. The Enable controls whether the output is a LOW or HIGH (enabled) or Tri-Stated (disabled).

- Tri-state outputs are typically used where multiple outputs share a signal or bus.

  Example; data outputs on memory devices are tri-state outputs. Control circuitry is used to ensure that only one device is enabled at any given time (to decode logic).

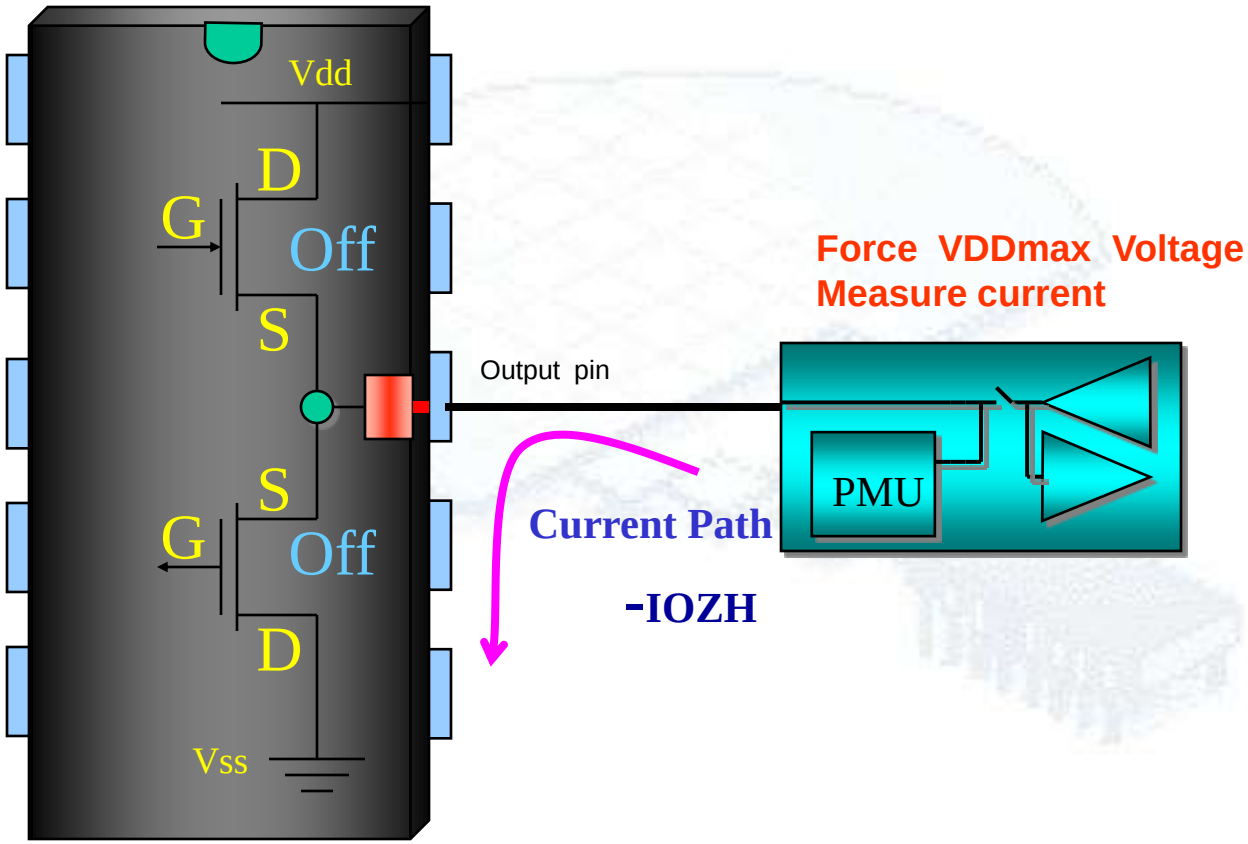
Why IOZ Test ?

- Measures the resistance from an output pin to ground / VDD.
- To confirm the bi-directional and high impedance outputs are capable of achieving a high impedance or off state.
- Identify processing problems in CMOS devices.

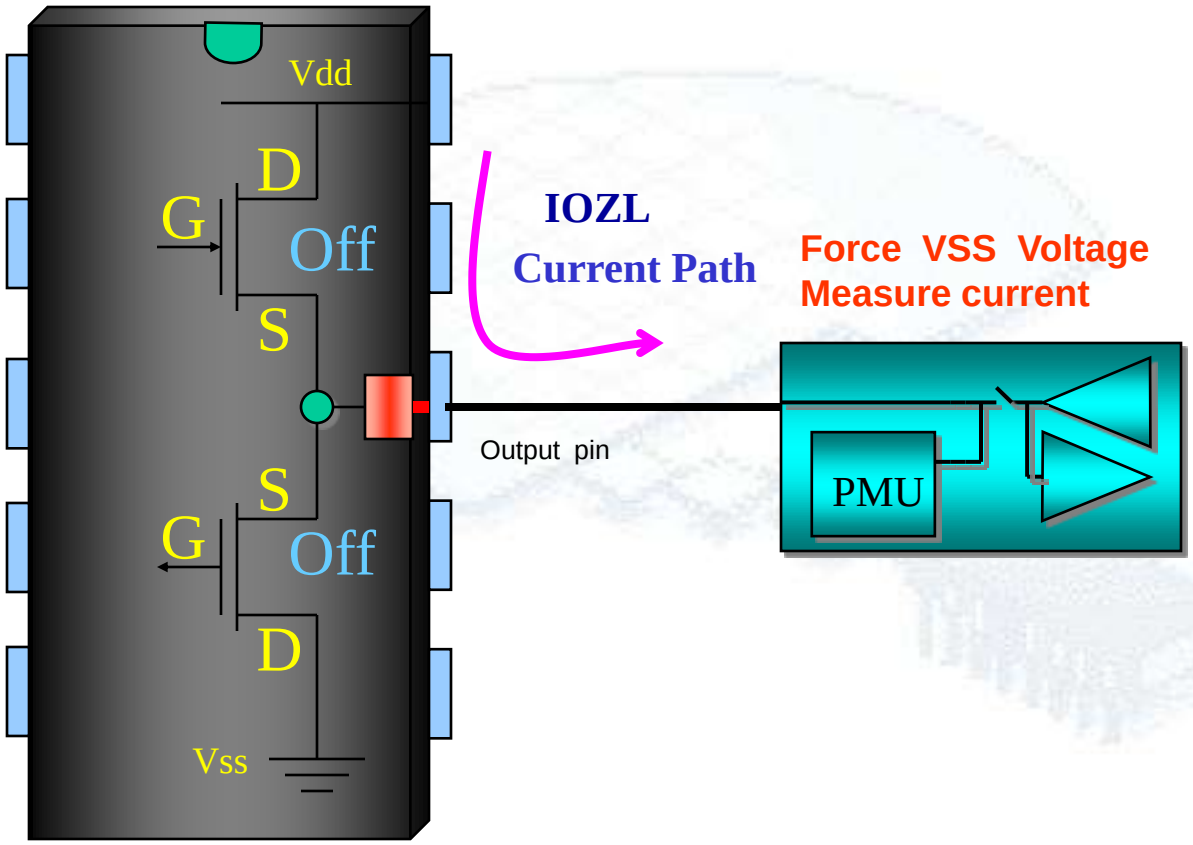
IOZL/IOZH Serial Test Method

- All output pins should be preconditioned to High impedance state.
- Use PMU to force High into all tristate pin individually and measure the current (IOZH) and compare it with the specification limits.
- Use PMU to force Low into all tristate pins individually and measure the current (IOZL) and compare it with specification limits.

IOZH Serial Test Method



IOZL Serial Test Method



IOZL/IOZH Parallel Test Method

- Most Test Systems today have per Pin PMU.
- Parallel measurements mean all high impedance outputs will be driven for Low simultaneously and measurement (IOZL) will be done.
- Similarly, all high impedance pins will be driven for High and measurement (IOZH) will be done.

Tri State Leakage Test Sample Datalog

Number	Site	Result	Test Name	Pin	Channel	Low limit	Measured	High limit	Force
250	0	PASS	Low_trileak_p2	p23	7	-2.0000 uA	-2.2912 nA	2.0000 uA	0.0000 V
251	0	PASS	Low_trileak_p2	p22	31	-2.0000 uA	-5.1700 nA	2.0000 uA	0.0000 V
252	0	PASS	Low_trileak_p2	p21	23	-2.0000 uA	-1.0839 nA	2.0000 uA	0.0000 V
253	0	PASS	Low_trileak_p2	p20	48	-2.0000 uA	-523.1774 pA	2.0000 uA	0.0000 V
254	0	PASS	Low_trileak_ctr	cs	4	-2.0000 uA	124.6501 pA	2.0000 uA	0.0000 V
255	0	FAIL	Low_trileak_ctr	prg	30	-2.0000 uA	-3.7916 uA		
256	0	PASS	Hi_Trileak_p2	p23	7	-2.0000 uA	3.7916 nA		
257	0	PASS	Hi_Trileak_p2	p22	31	-2.0000 uA	10.9652 nA	2.0000 uA	5.5000 V
258	0	FAIL	Hi_Trileak_p2	p21	23	-2.0000 uA	4.4392 uA		
259	0	PASS	Hi_Trileak_p2	p20	48	-2.0000 uA	-2.3655 pA		
260	0	PASS	Hi_Trileak_ctr	cs	4	-2.0000 uA	531.6501 pA	2.0000 uA	5.5000 V
261	0	PASS	Hi_Trileak_ctr	prg	30	-2.0000 uA	124.2792 pA	2.0000 uA	5.5000 V

Fail IOZL

Fail IOZH

In the above example, pin PRG failed due to tri state Low leakage & P21 failed due to tri state High leakage

Revised 8/8/2007

IOS Test

- **IOS - Output Short Circuit Current**

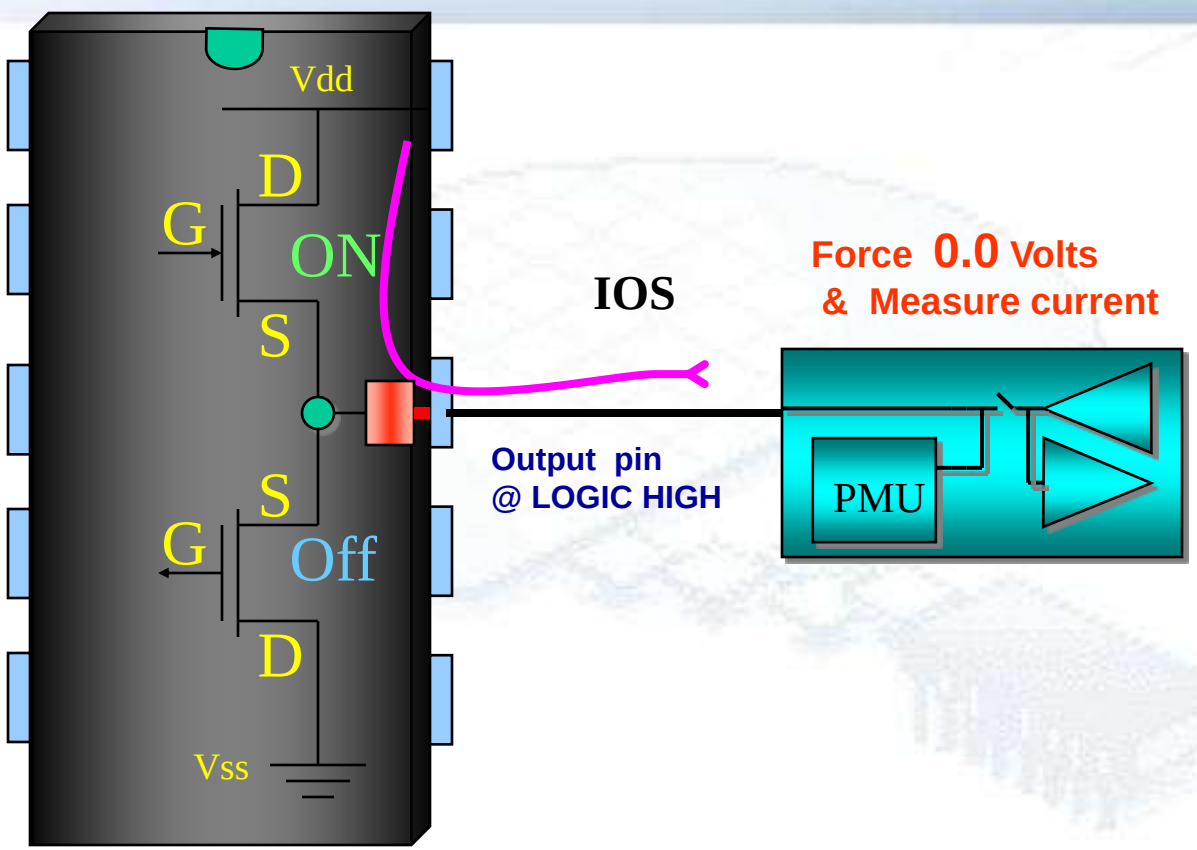
- This is the current produced by the output during short circuit condition.

- IOS usually specified in the devices specification.

- IOS test is used to measure the output pins steady state impedance.

- It is the max current measured while the device output is in logic 1(output High state) and 0 volts applied to the output.

IOS Test Method

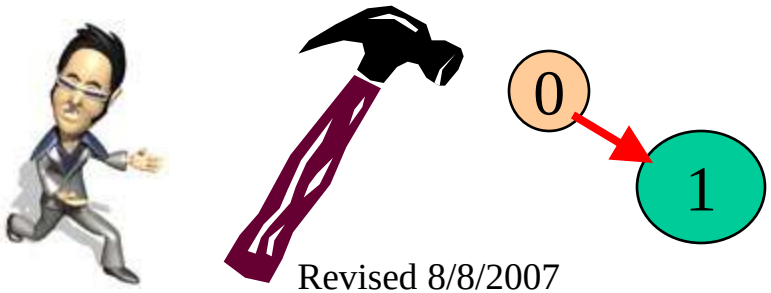


- Precondition Output pin to output logic High.
- Force 0 Volt from PMU to this pin. Add delay/wait time of 1 to 5ms
- Measure resultant current and compare against the IOS test limits .

Revised 8/8/2007

IOS Test Method

- All the outputs of DUT should be preconditioned to logic high.
- PMU will drive 0V and resultant current will be measured and compared to the specification.
- This is repeated for all output pins.
- Hot switching should be avoided when performing IOS Test.



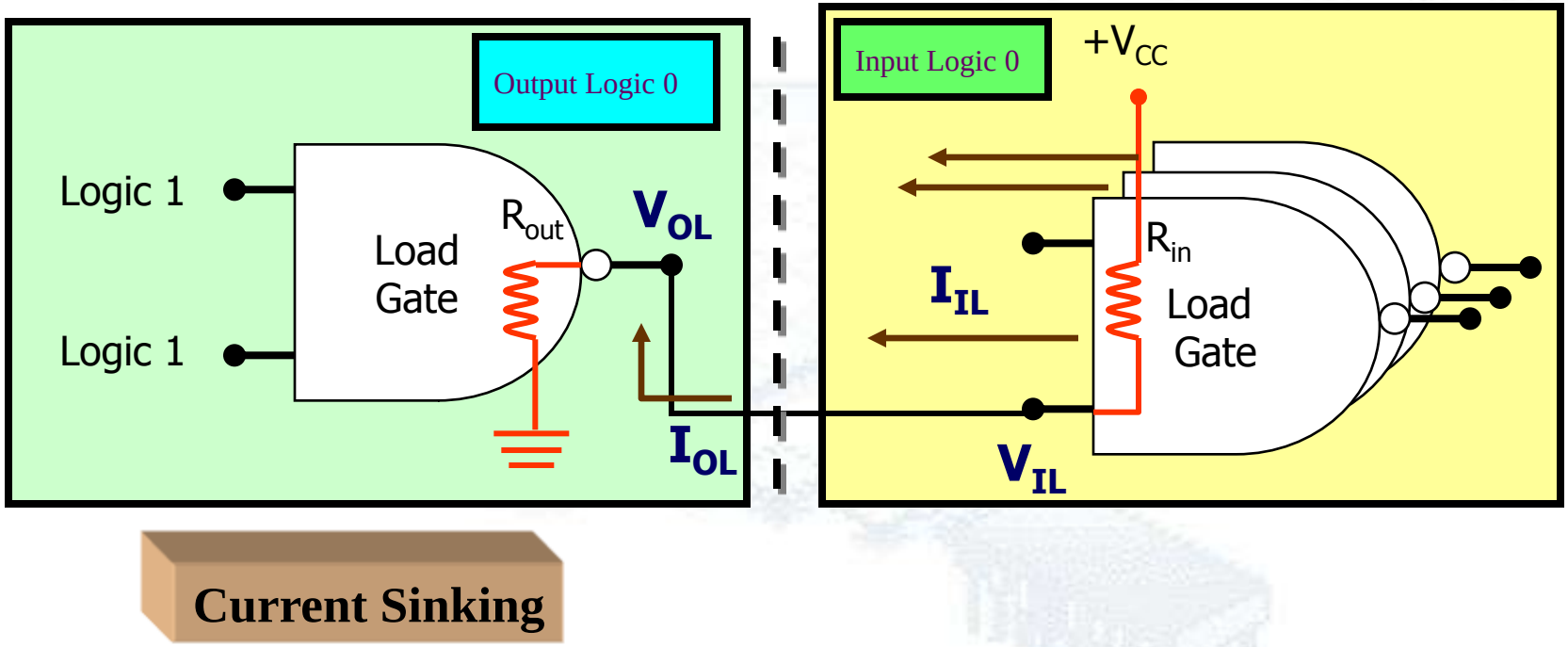
VOL/IOL

- VOL represents the maximum output voltage when the output is low.
- IOL represents the maximum sinking current capability when the output is in low state

Why VOL/IOL Test ?

- Measures the resistance of an output pin when the logic is 0.
- Insures that output will provide IOL without exceeding the VOL voltage.
- Device output pin must sink at least the specified current and stay in correct logic state.

VOL/IOL



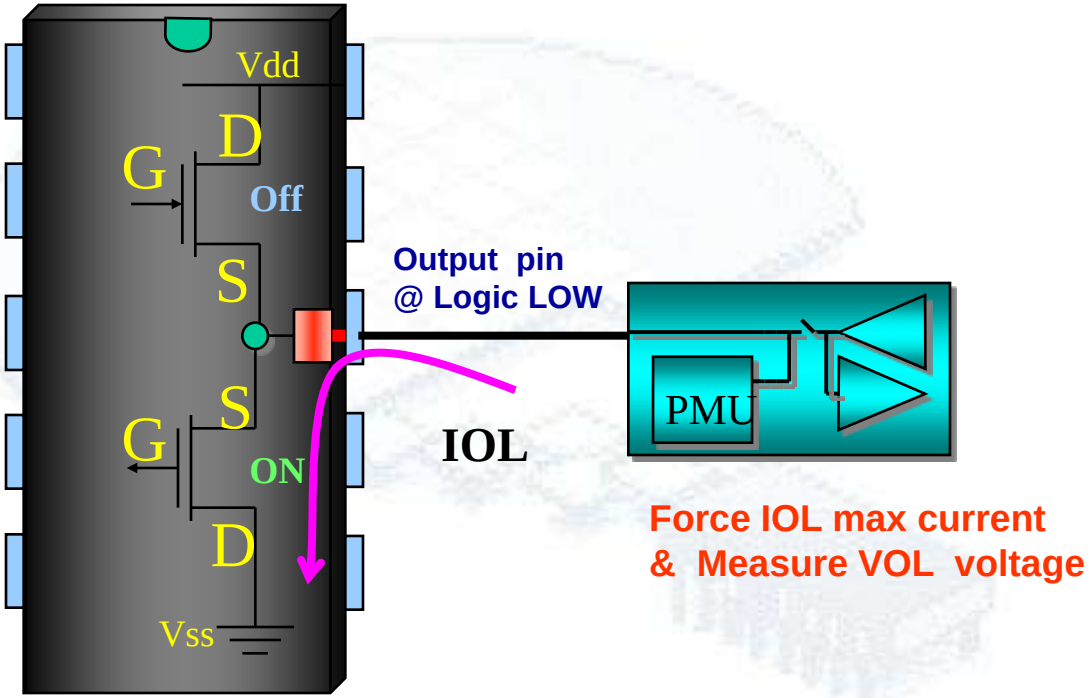
Current Sinking

Test Method for VOL/IOL

- Device output pins are preconditioned for logic low state.
- PMU is connected to pin under test and IOL current is injected and the resultant voltage is measured and compared with the specification.
- Typical specification

  VOL @vddmin = 0.4 V @ IOL = 8.0 ma

Test Method for VOL/IOL



Vdd minimum is the worst case for this test.

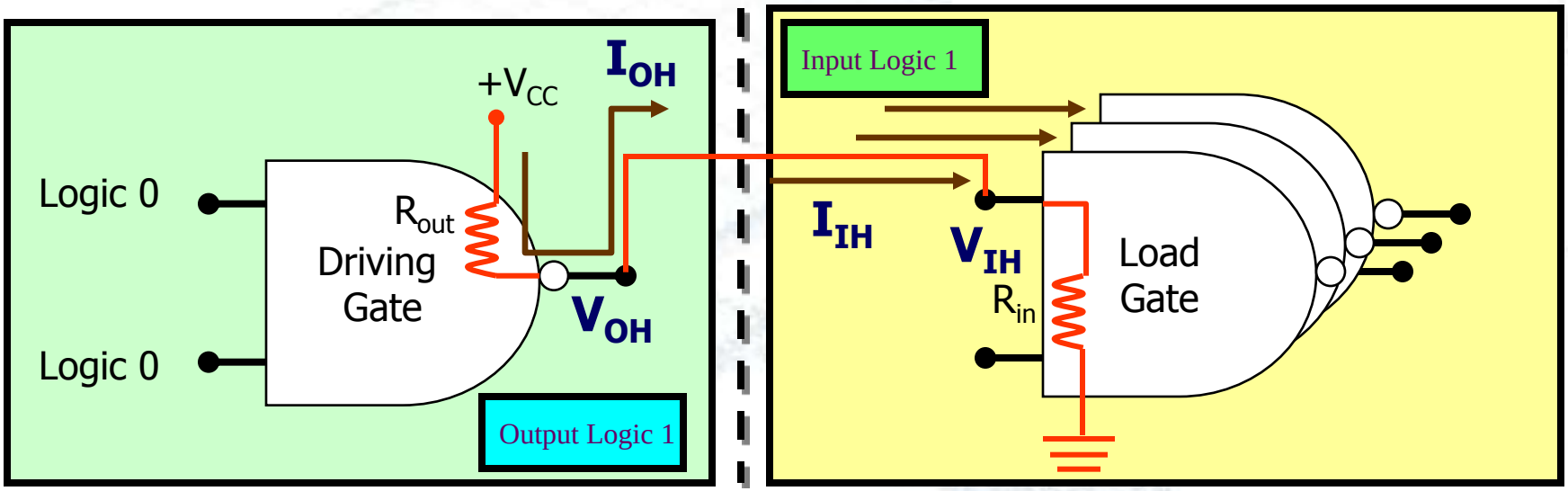
VOH/IOH

- VOH represents the minimum output voltage when the output is high.
- IOH represents the maximum sourcing current capability when the output is in high state.

Why VOH/IOH Test ?

- Measures the resistance of an output pin when the logic is 1.
- Insures that output will provide IOH without exceeding the VOH limit.
- Device output pins must source at least the specified current and stay in correct logic state.

VOH/IOH



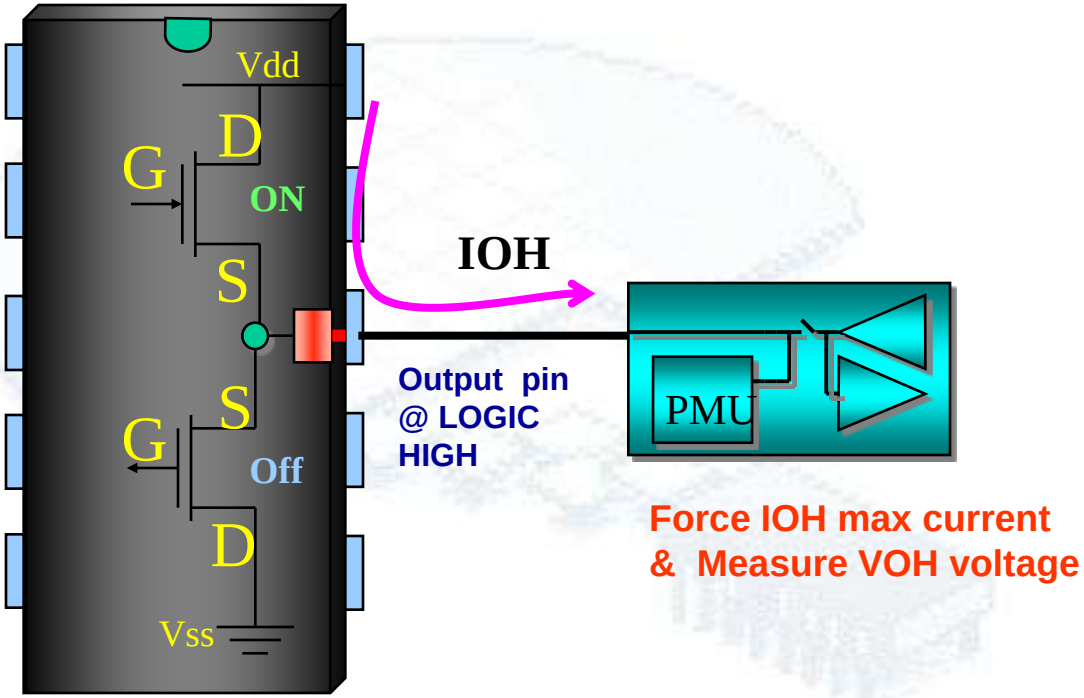
Current Sourcing

Test Method for VOH/IOH

- Device output pins are preconditioned for logic high state.
- PMU is connected to pin under test and IOH current is injected and the resultant voltage is measured and compared with the specification.
- Typical specification

  VOH @vddmin = 2.4 V @ IOH = - 5.0 ma

Test Method for VOH/IOH



Vdd minimum is the worst case for this test.

Output Fanout

- The *fanout* of a logic gate is the number of inputs that the gate can drive without exceeding its worst-case loading specifications.

- CMOS devices fanout is mostly depending on the speed we operate as it is high input impedance device.

Output Fanout

Fanout must be examined for both possible output states.

- IOLMAX

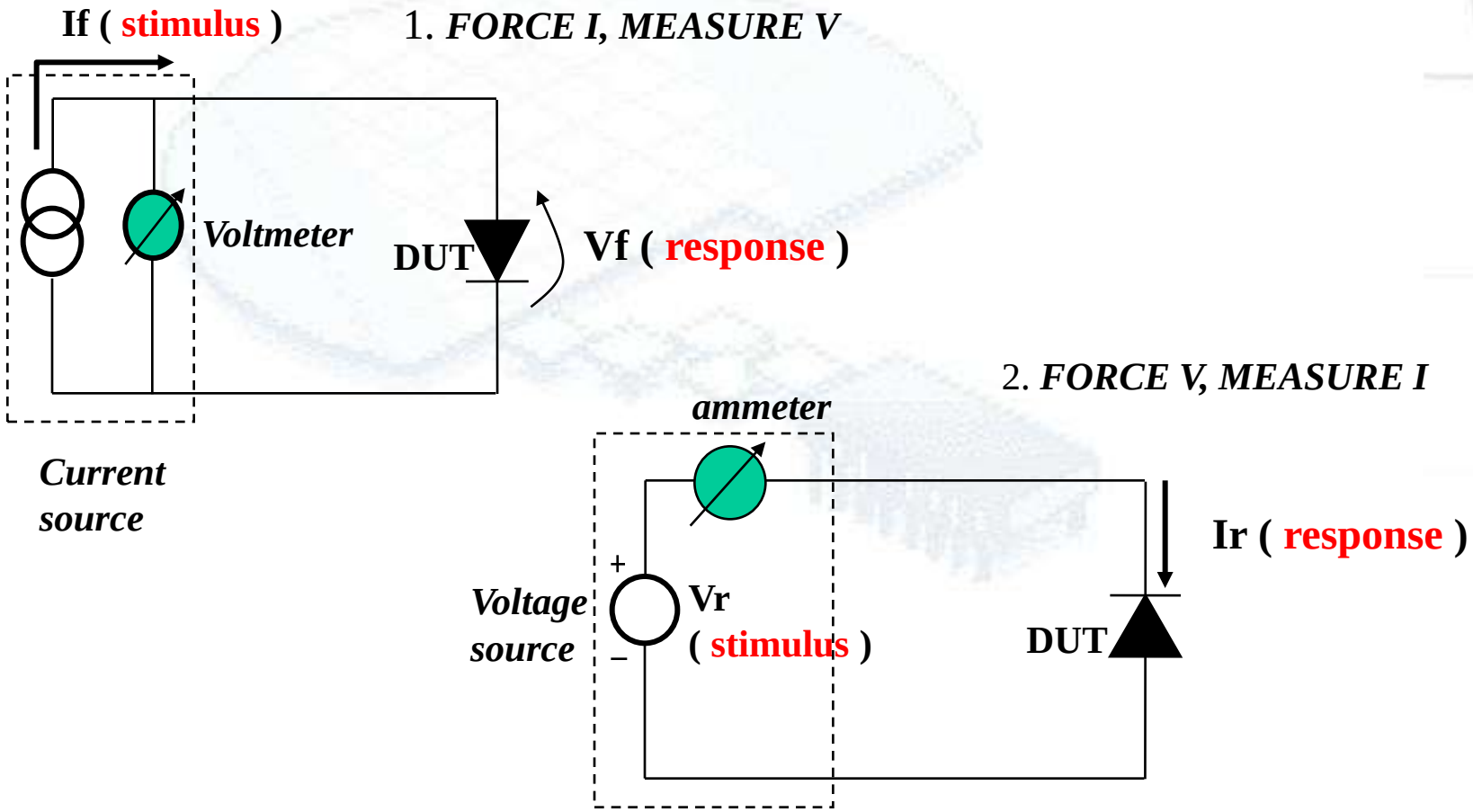
  The maximum current that the output can sink in the LOW state while still maintaining an output voltage no greater then VOLMAX.

- IOHMAX

  The maximum current that the output can source in the HIGH state while still maintaining an output voltage no less then VOHMIN.

ATE DC SUBSYSTEM
VOLTAGE/CURRENT (VI) SOURCE

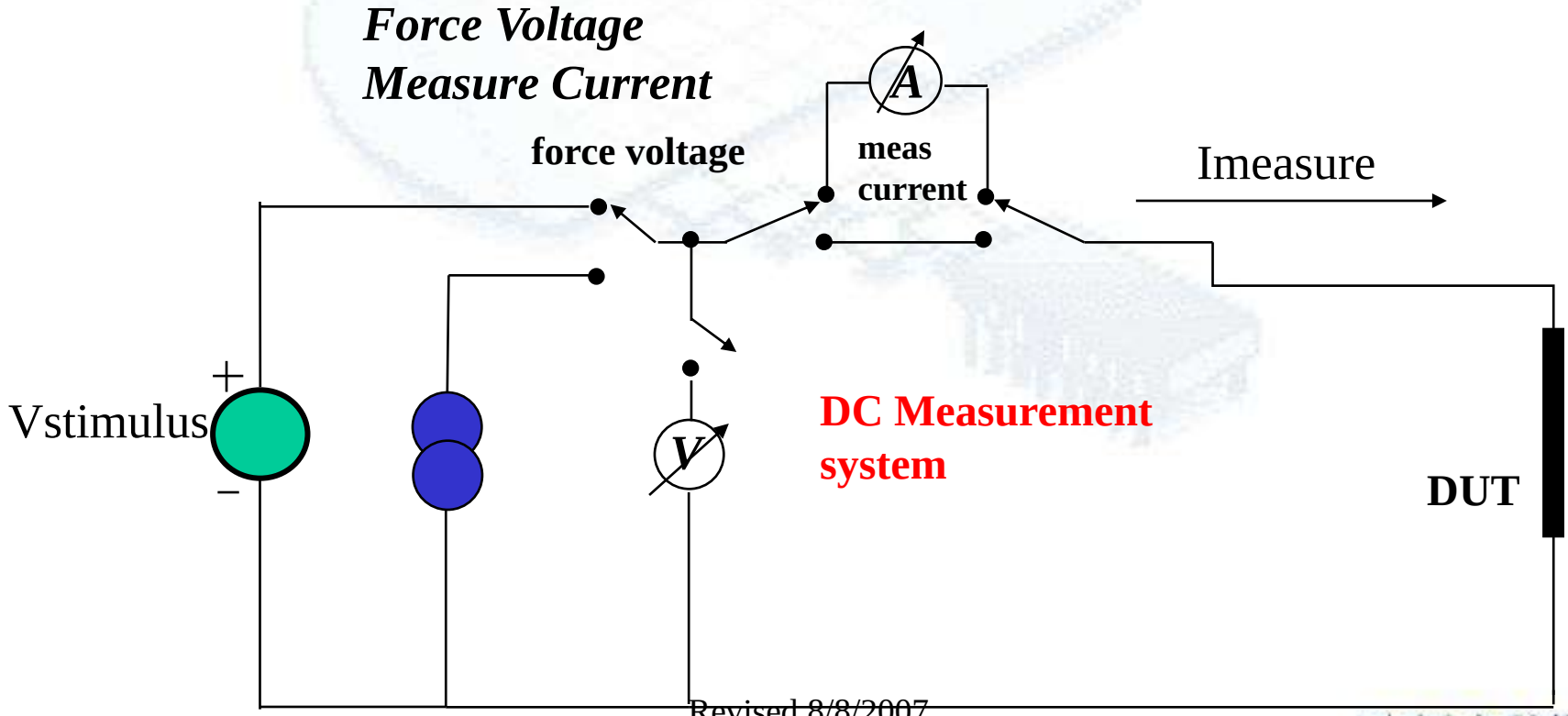
To generalize DC testing, 2 configurations exist:



VOLTAGE/CURRENT (VI) SOURCE

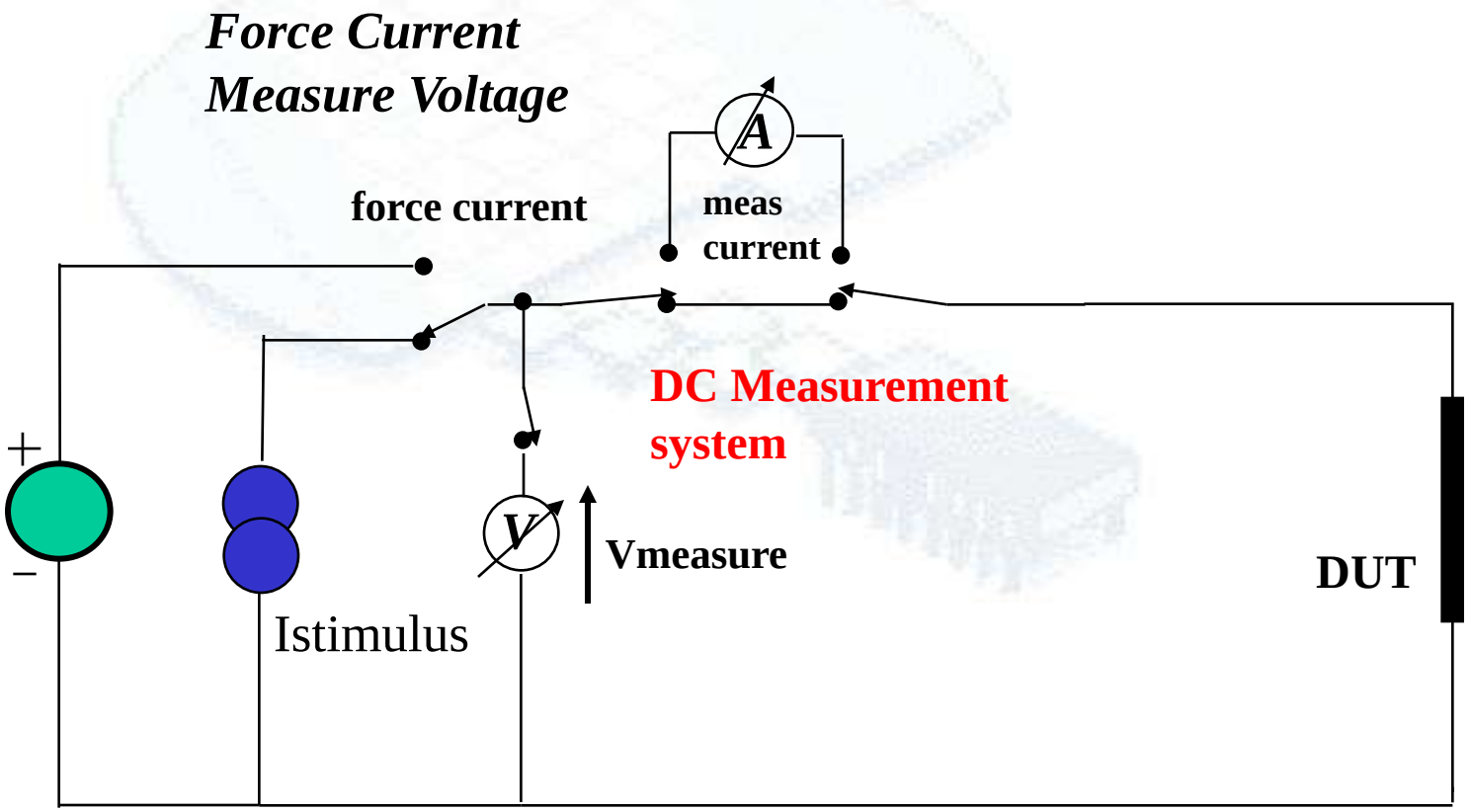
The 2 configurations of DC tests calls for a DC source capable of both modes, the Voltage/Current source or VI source.

A generalized form of the VI source in Force V measure I mode:



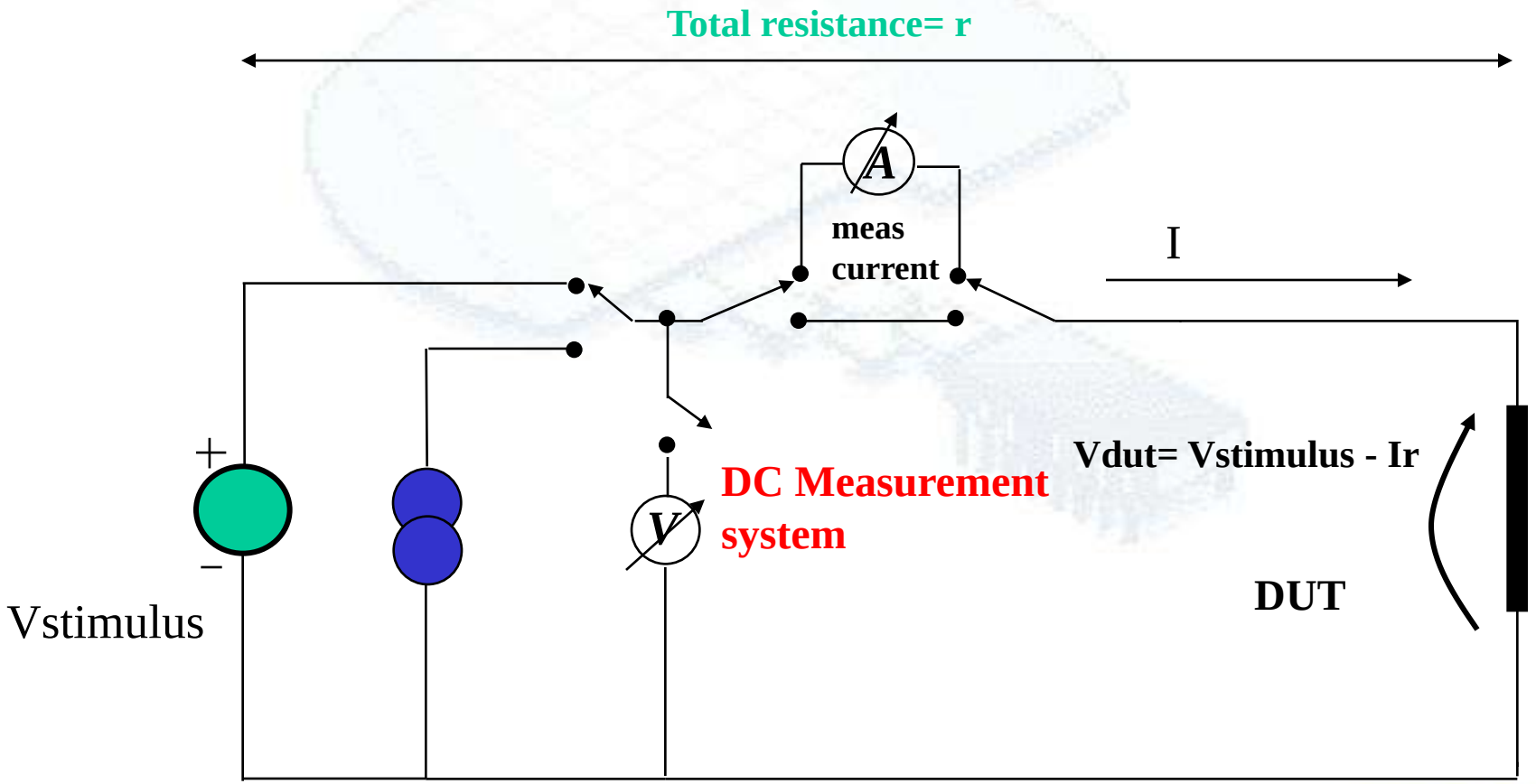
VOLTAGE/CURRENT (VI) SOURCE

A generalized form of the VI source in Force I measure V mode:



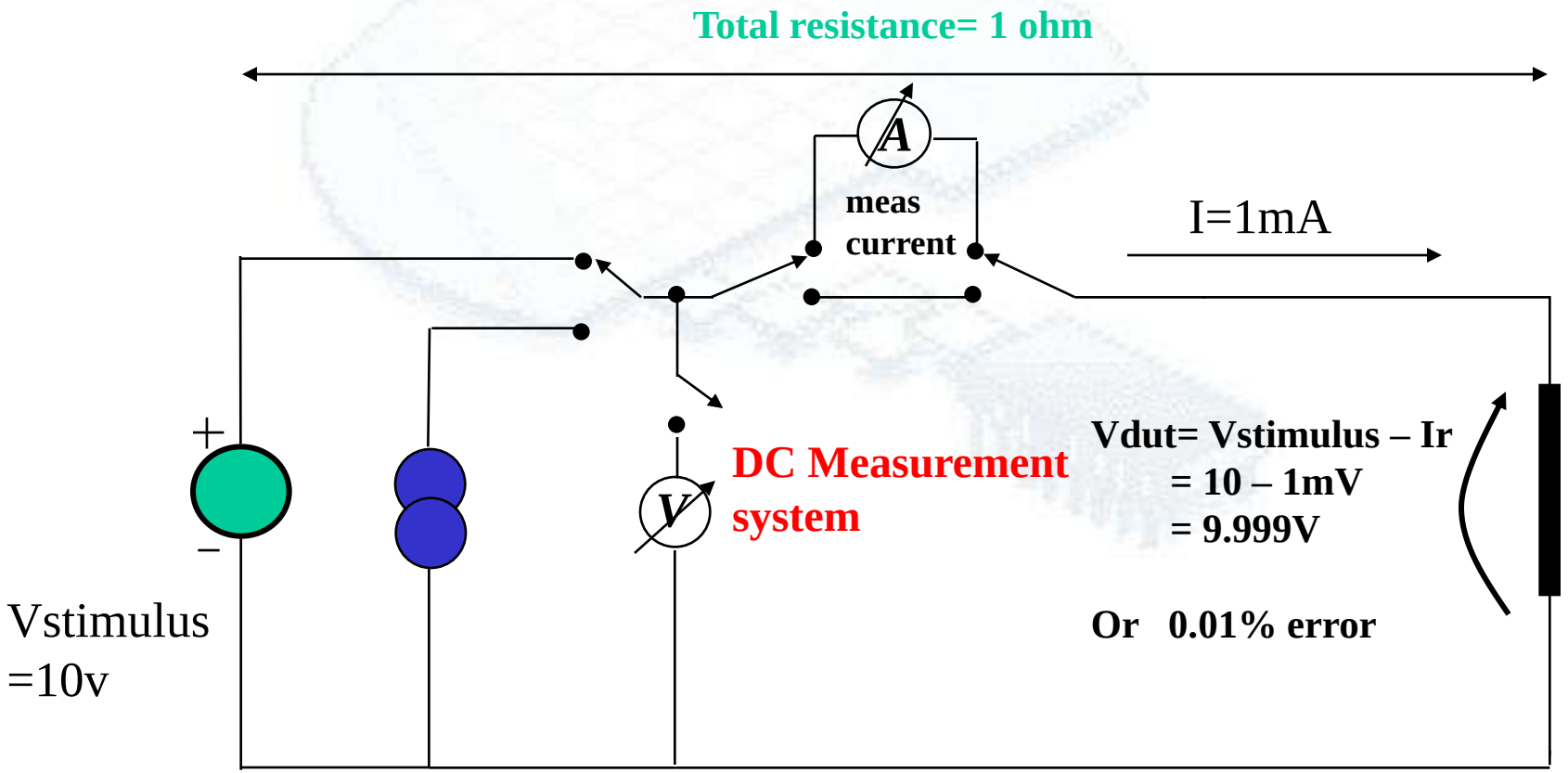
KELVIN CONNECTION CONCEPT

Inaccuracy of actual voltage delivered across the DUT arise due to inherent resistance in the connection between the voltage source and the DUT:



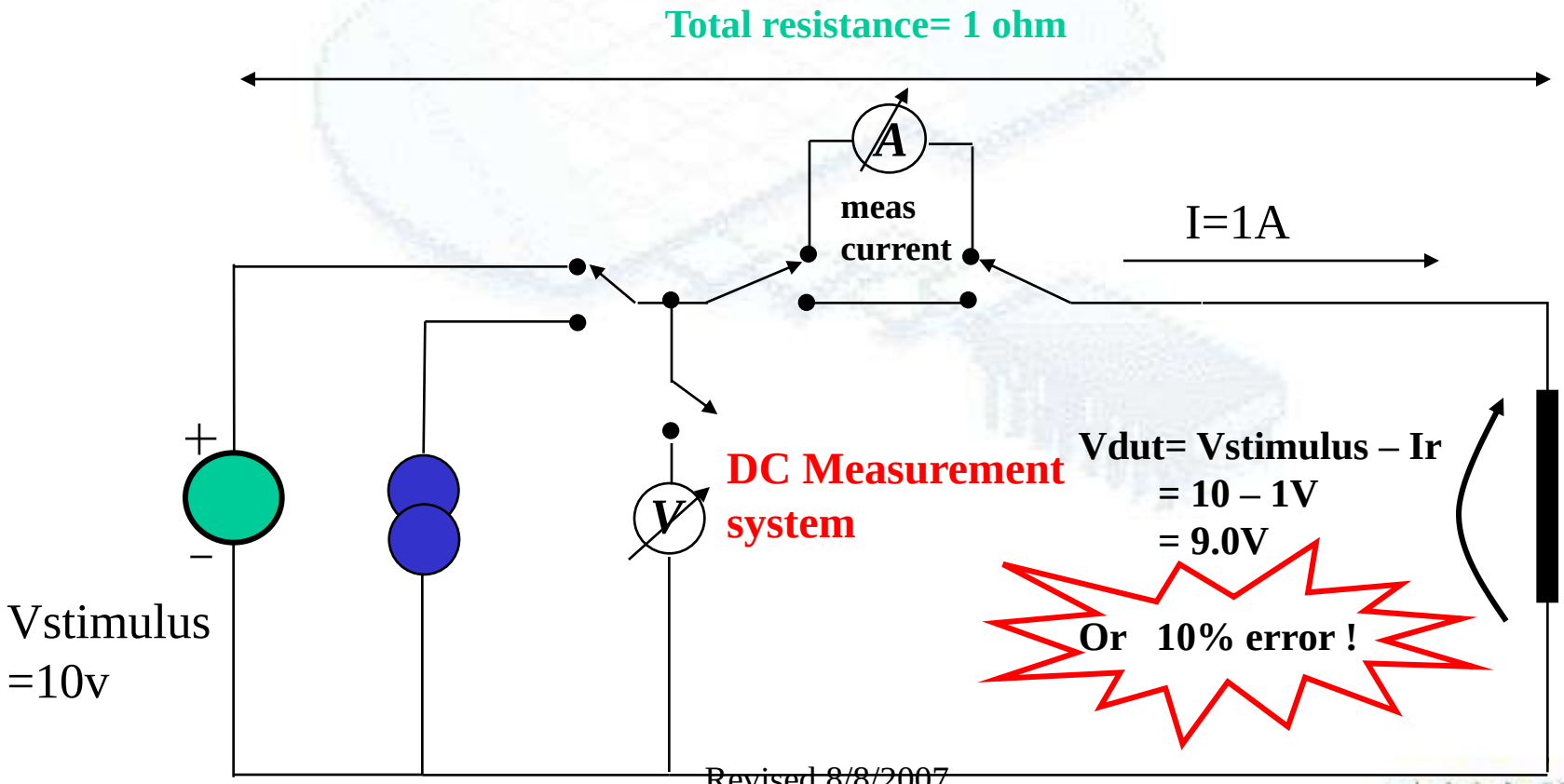
KELVIN CONNECTION CONCEPT

Vdut error is not very apparent for low currents:



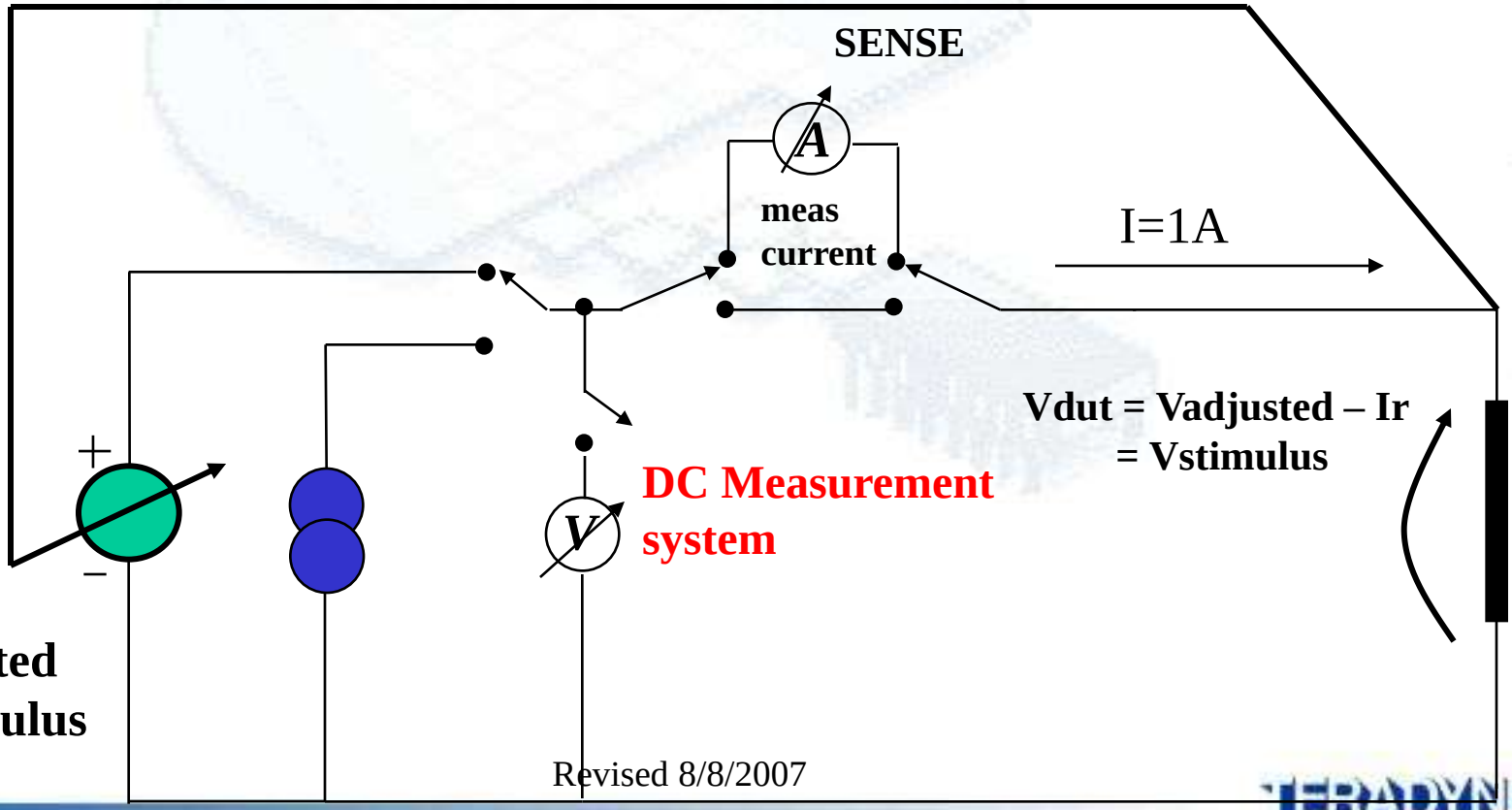
KELVIN CONNECTION CONCEPT

Vdut error IS apparent for higher currents:



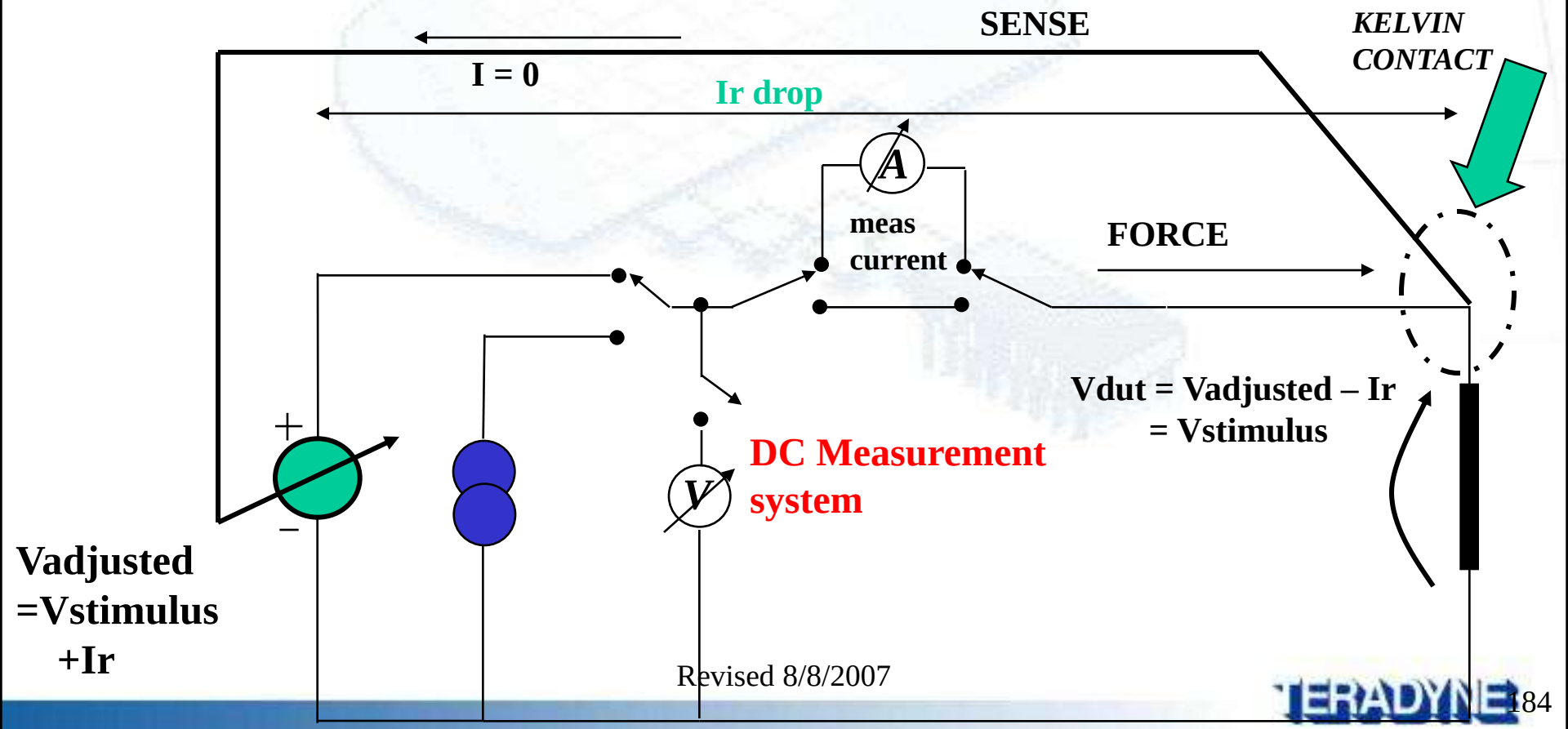
KELVIN CONNECTION CONCEPT

Ir error is eliminated by employing a separate conductor that provides feedback to the voltage source's error nulling circuitry.
This feedback conductor is called the SENSE line:



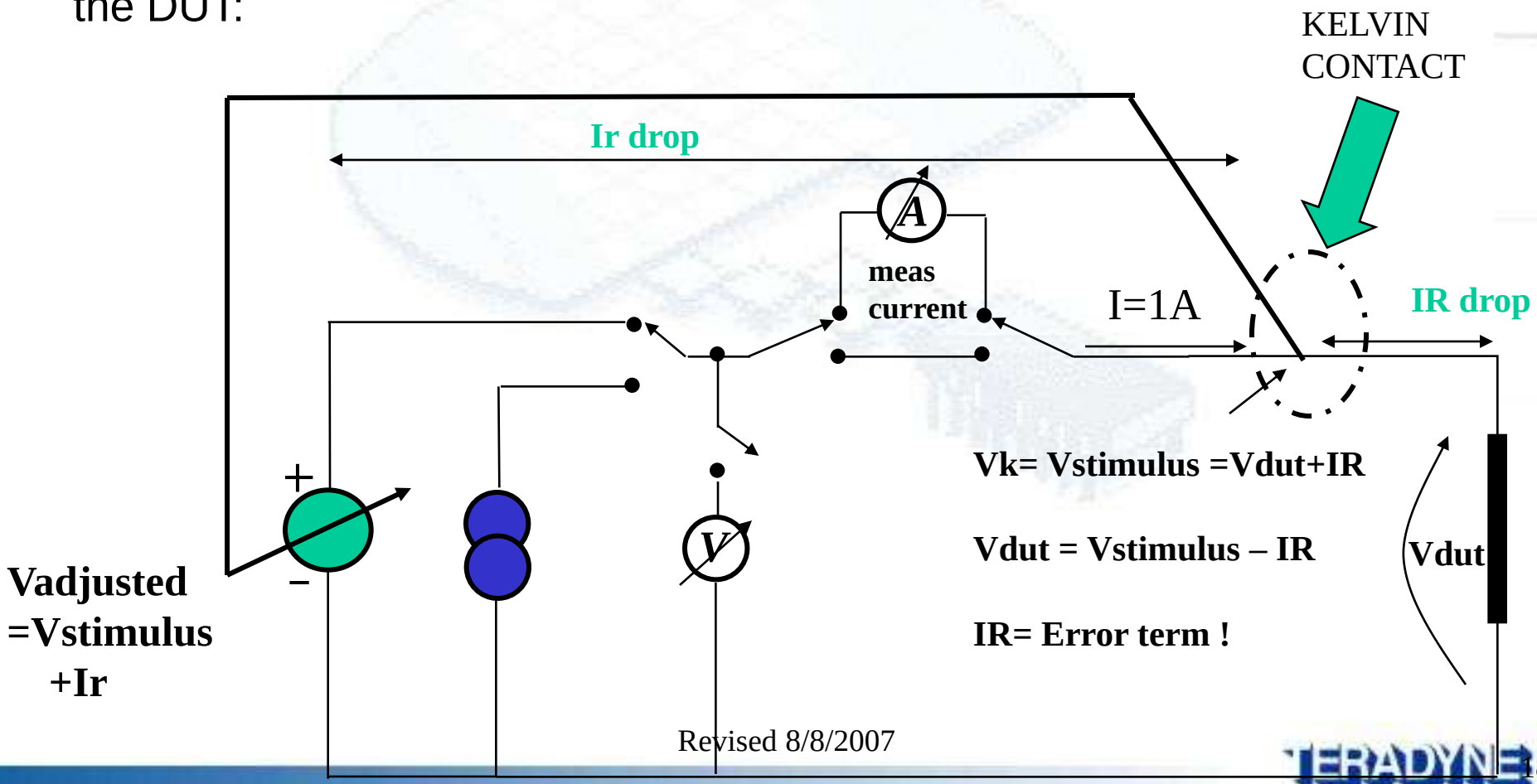
KELVIN CONNECTION CONCEPT

The FORCE line is the current carrying line.The SENSE line does NOT carry current as it feeds-back into a high impedance junction (OpAmp input). The SENSE and FORCE lines are separate and meet ONLY at the DUT pin. This is called the KELVIN CONTACT point.



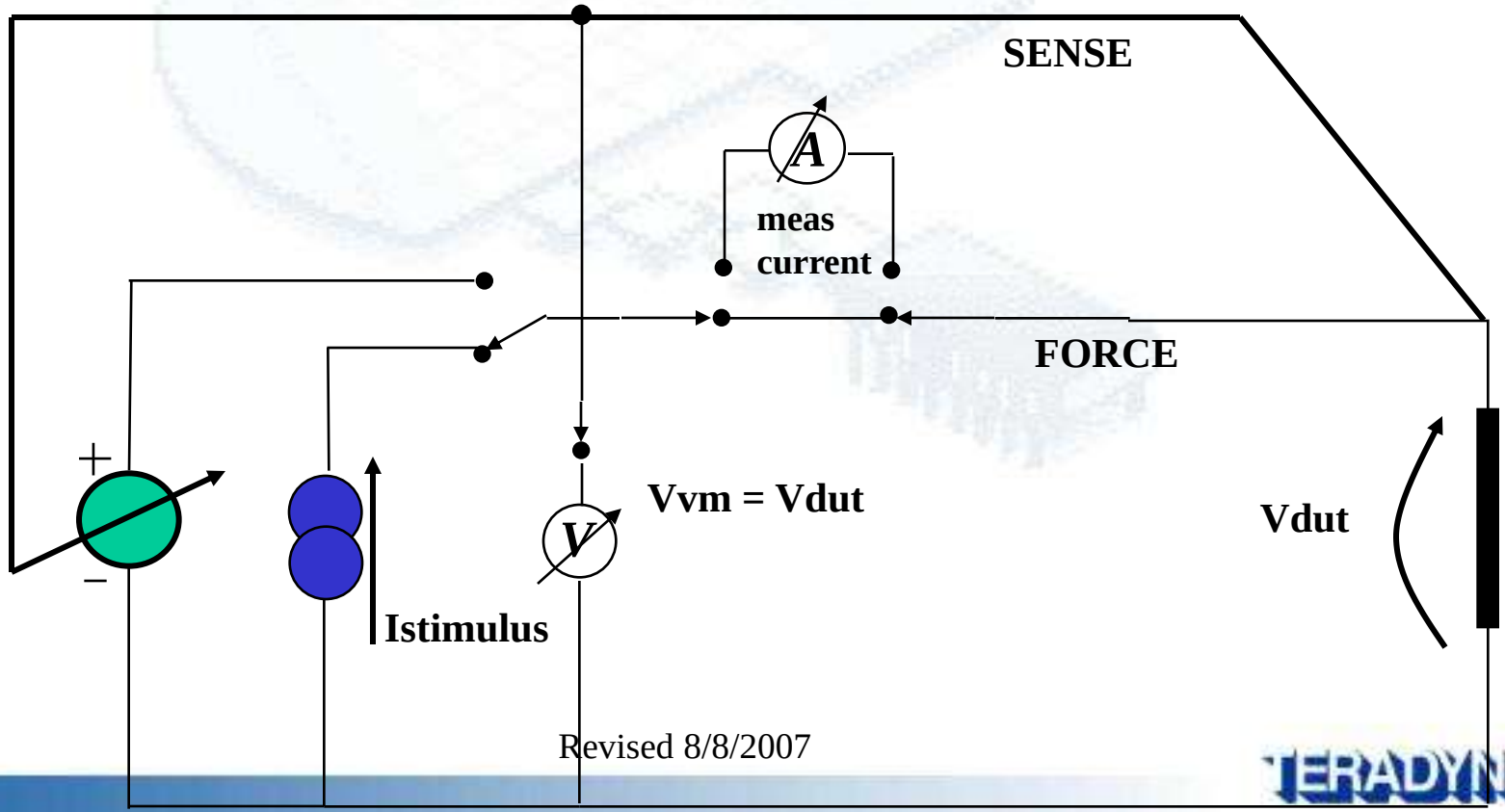
KELVIN CONNECTION CONCEPT

It is very important that the KELVIN CONTACT point is as close to the DUT leads as possible to ensure accuracy of required voltage across the DUT:



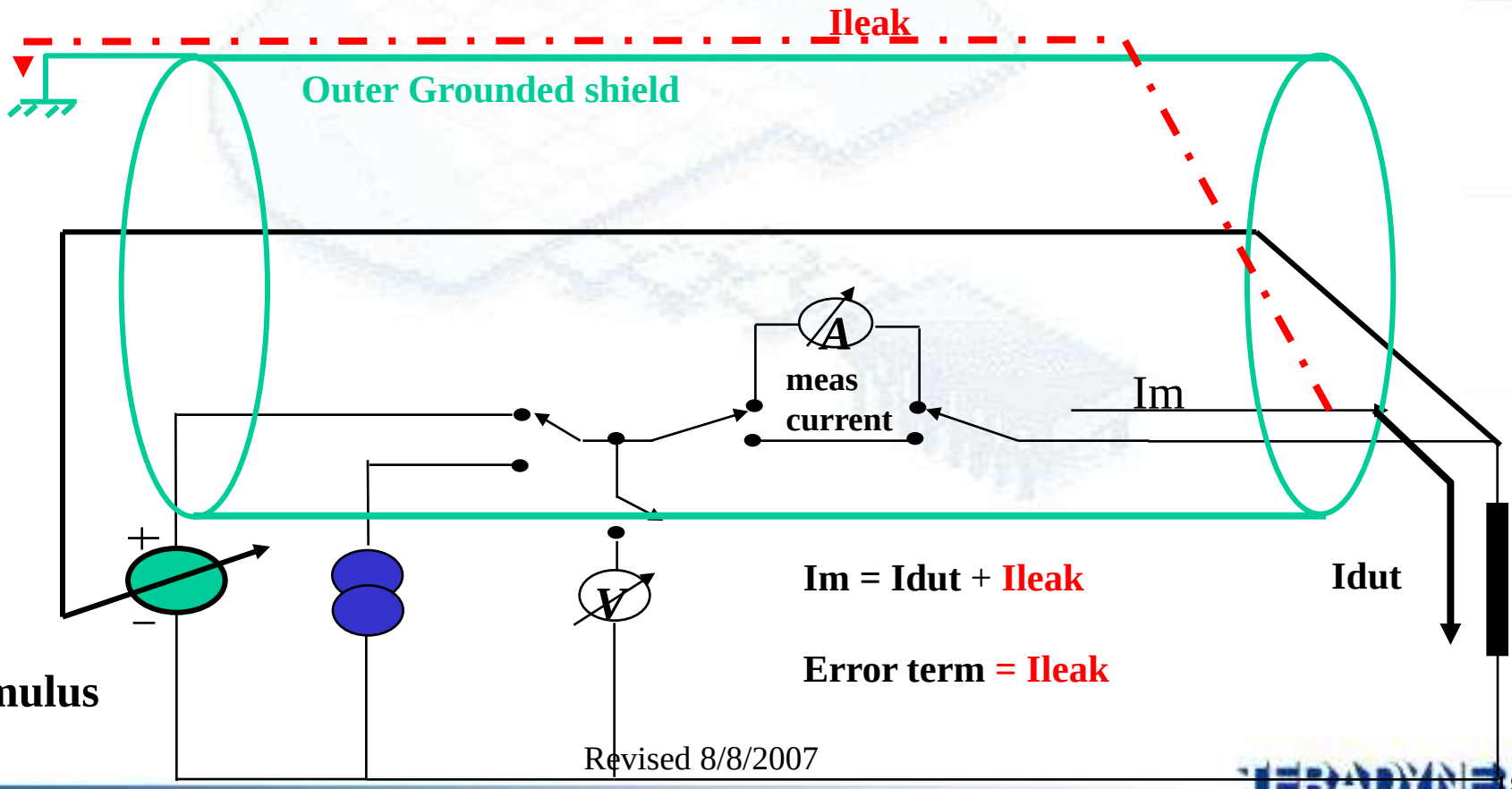
KELVIN CONNECTION CONCEPT

The KELVIN connection is also required for FORCE I, MEASURE V configuration. The Voltmeter measures the SENSE line since it carries virtually no current. Again, the KELVIN CONTACT point must be closest to the DUT for accuracy.



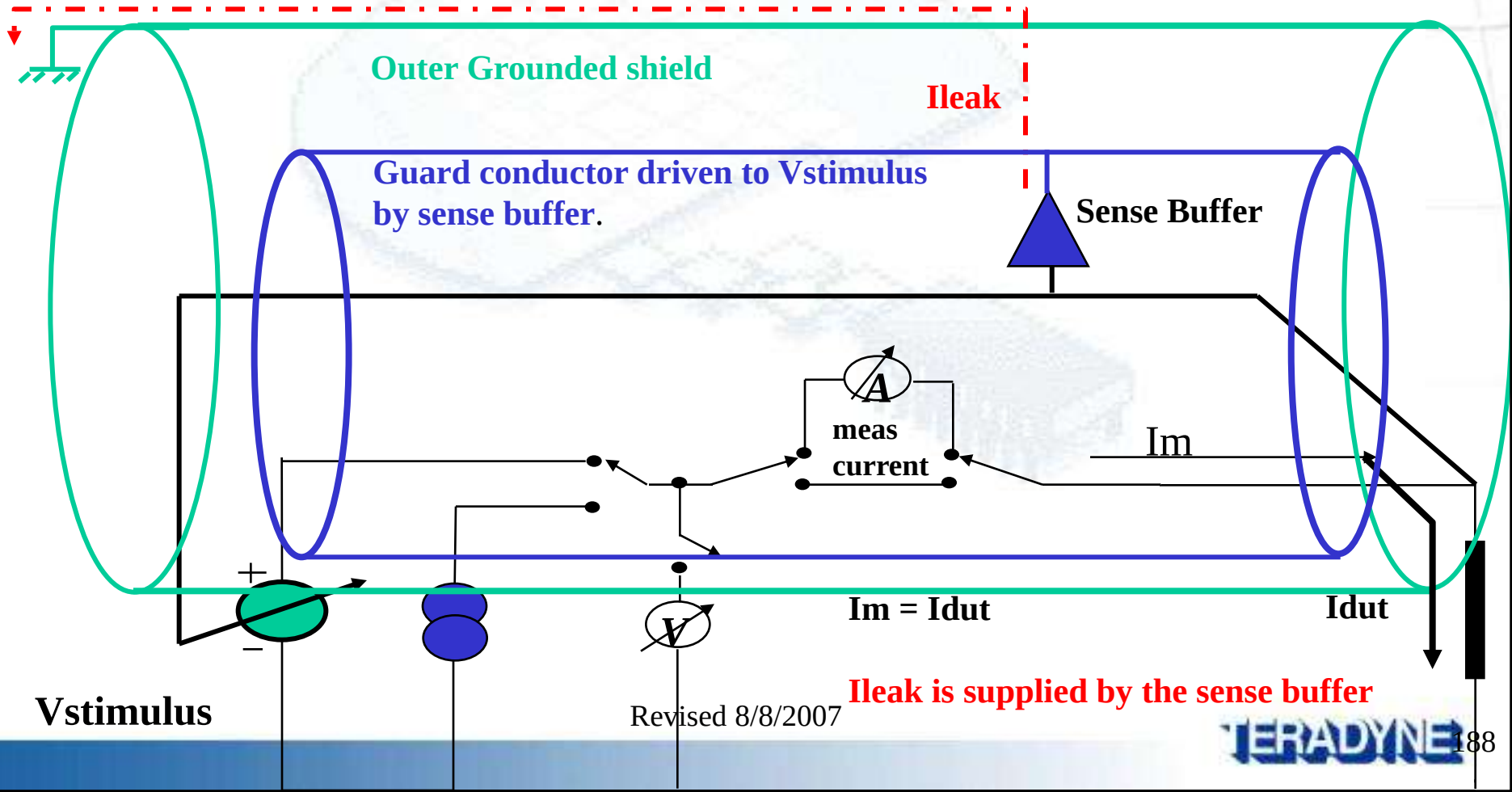
GUARD CONCEPT

When measuring currents in the micro or nano amp range, the measured current, Im will include leakage due to leaky currents thru the cable's dielectric to the grounded shield.The dielectric is only a few megaohms.



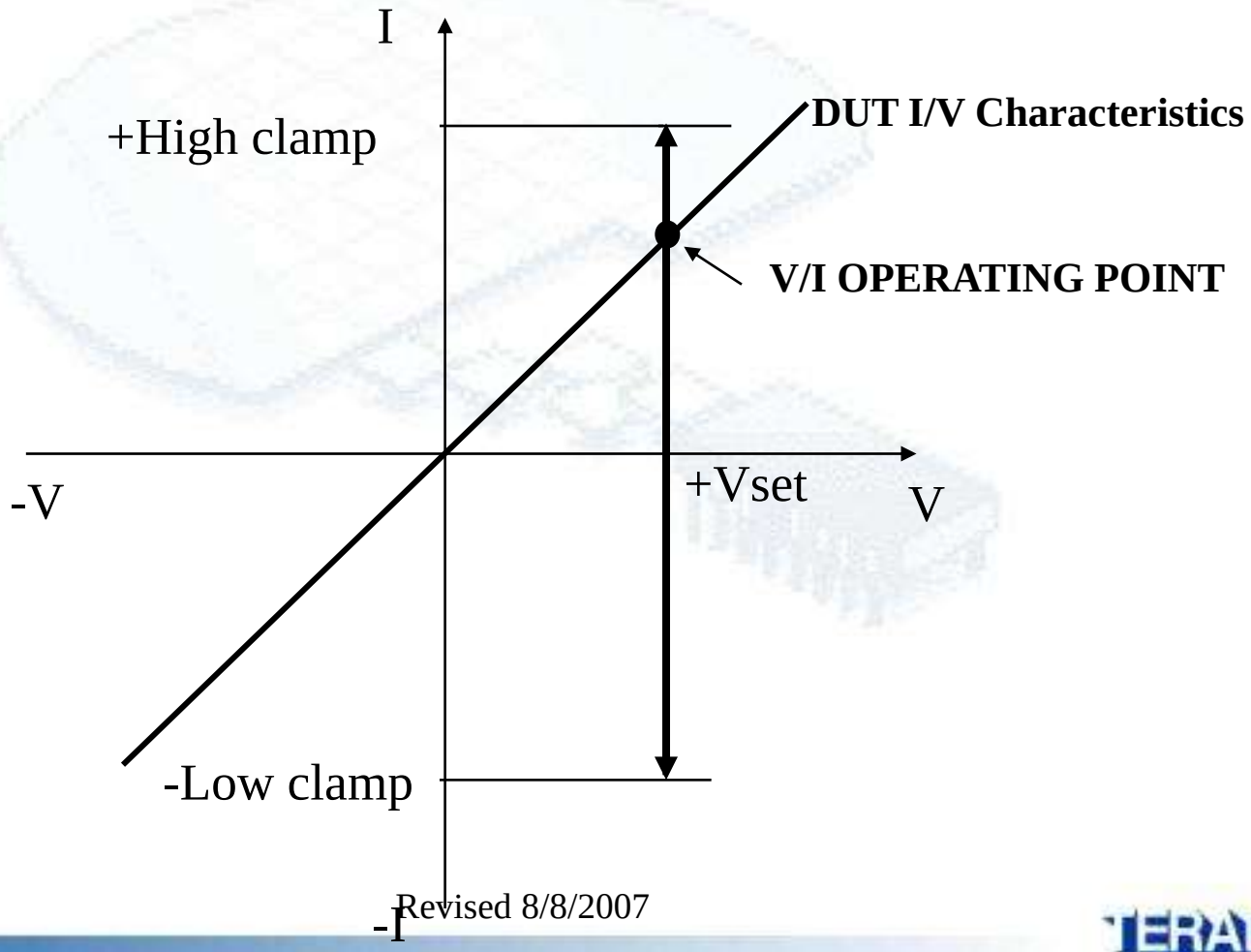
GUARD CONCEPT

The guard is a floating conductor that surrounds the Force and Sense leads and is driven by the sense voltage.The Ileak is now contributed by the sense buffer instead of the VI source.Im will be only Idut.



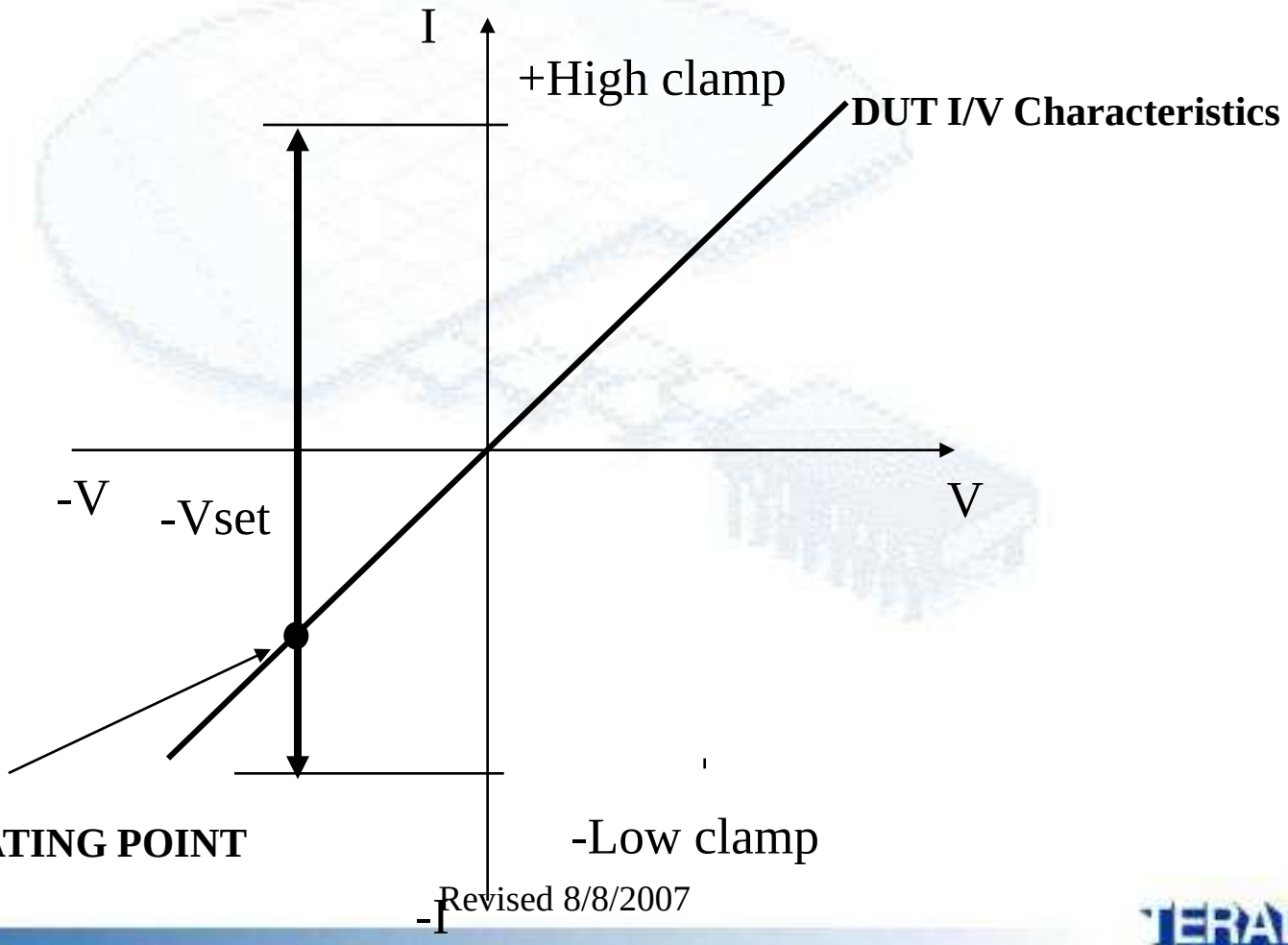
VOLTAGE/CURRENT (VI) SOURCE

The Voltage Source: The intercept point between the load line and the VI Operating line is the operating point of the VI.



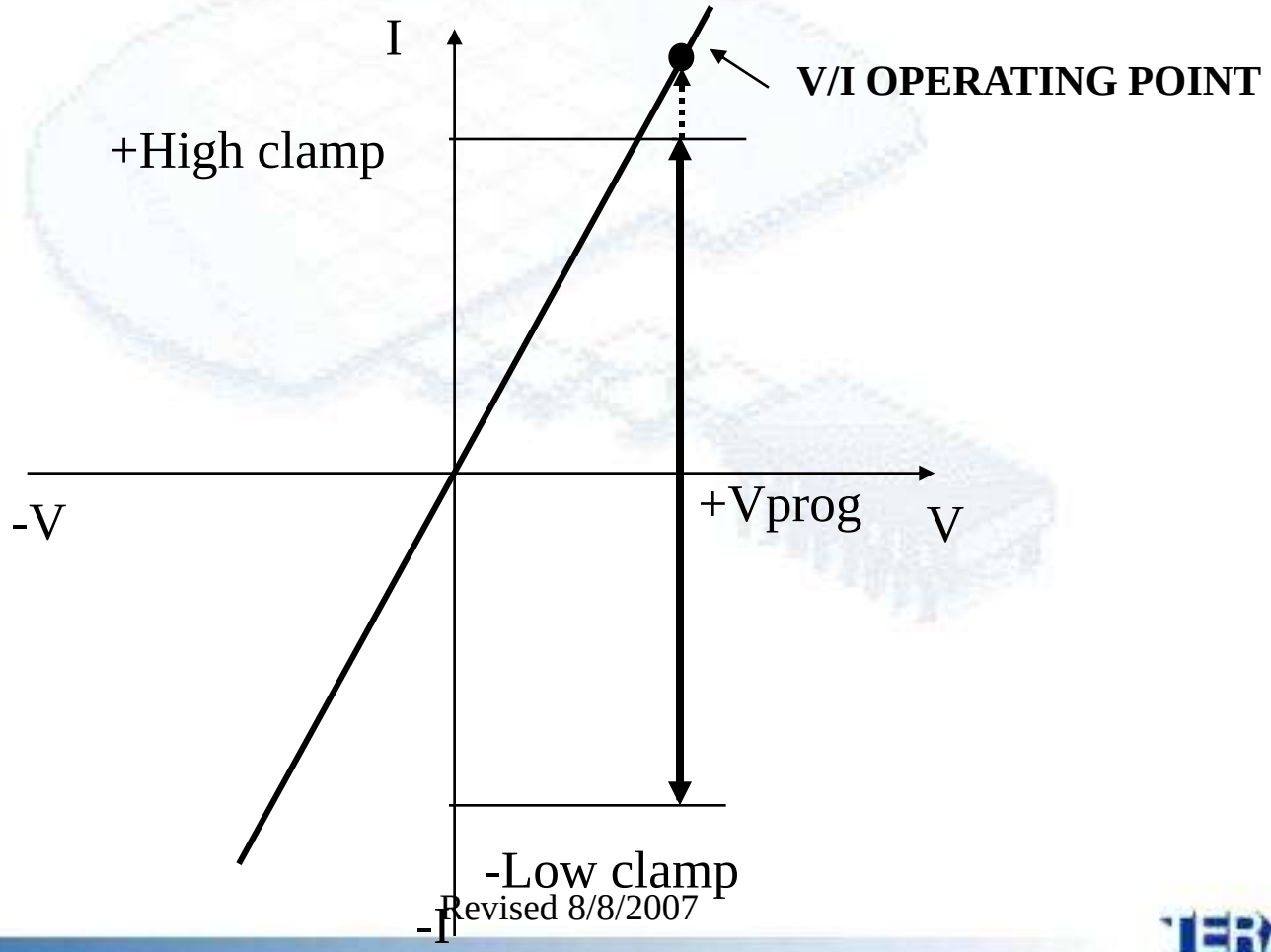
VOLTAGE/CURRENT (VI) SOURCE

The Voltage Source: The VI source can operate in negative Voltage and negative current mode as well.



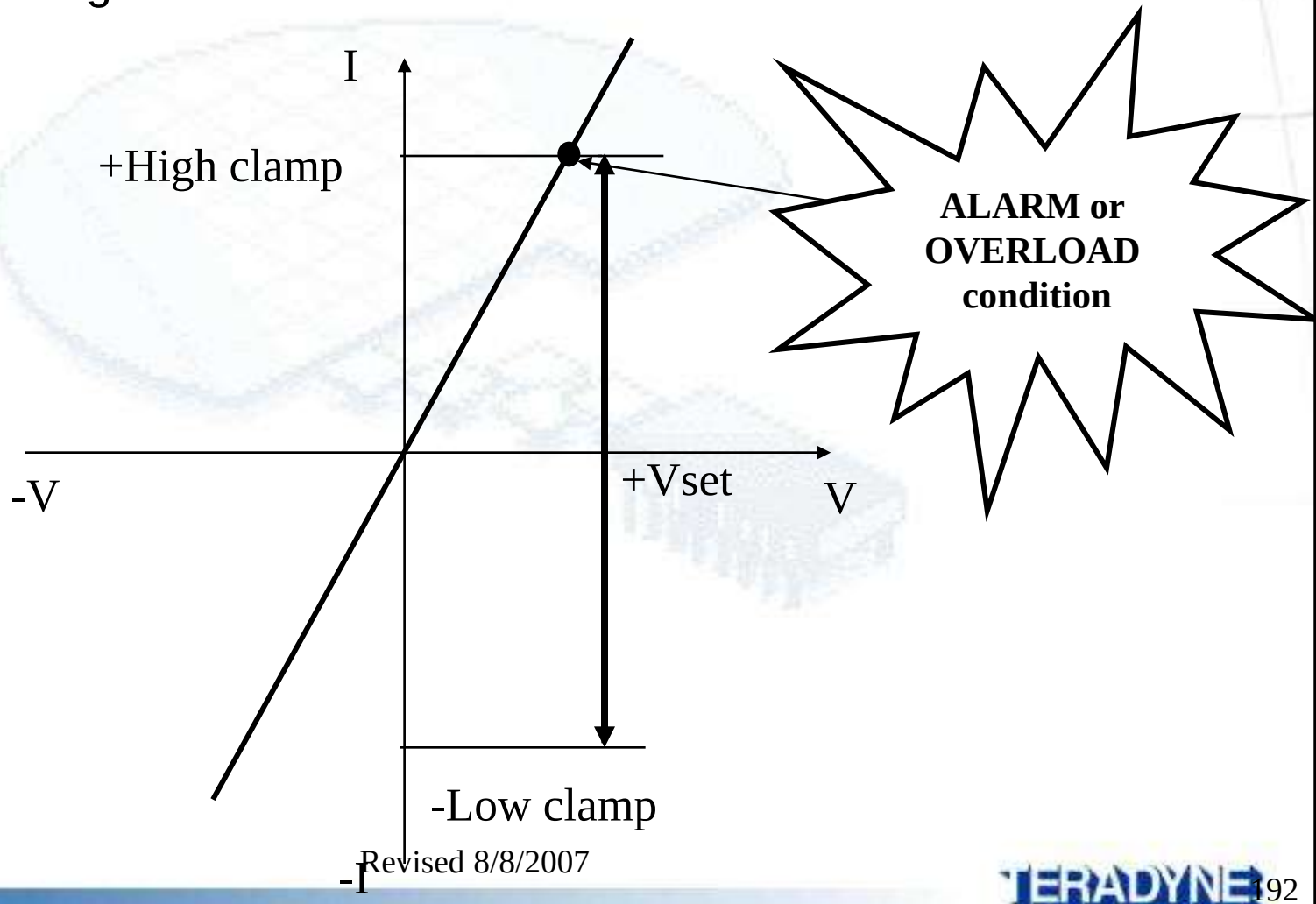
VOLTAGE/CURRENT (VI) SOURCE

The Voltage Source: What if the operating point is over the I clamp?



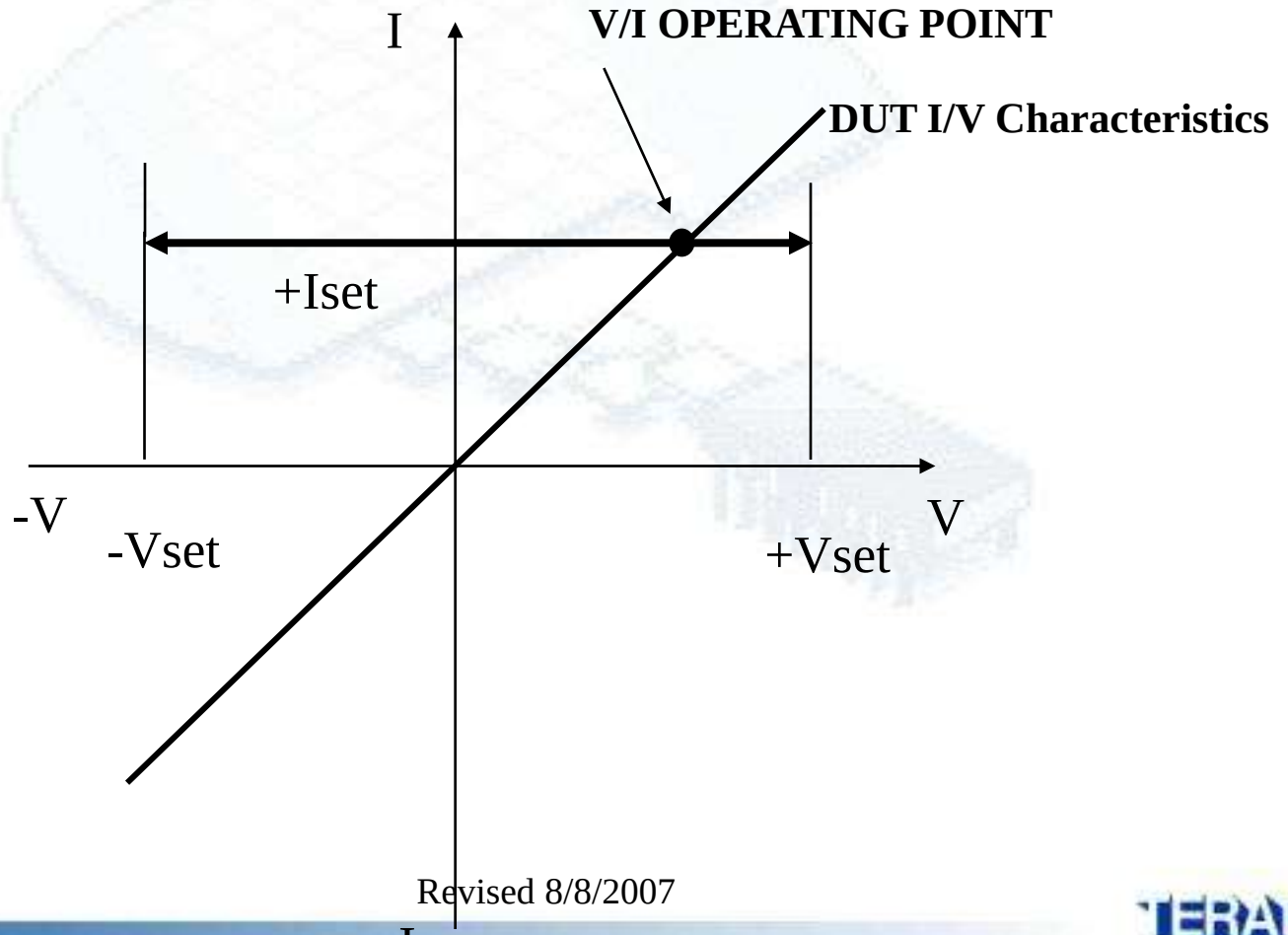
VOLTAGE/CURRENT (VI) SOURCE

The Voltage Source: ALARM in force V mode.



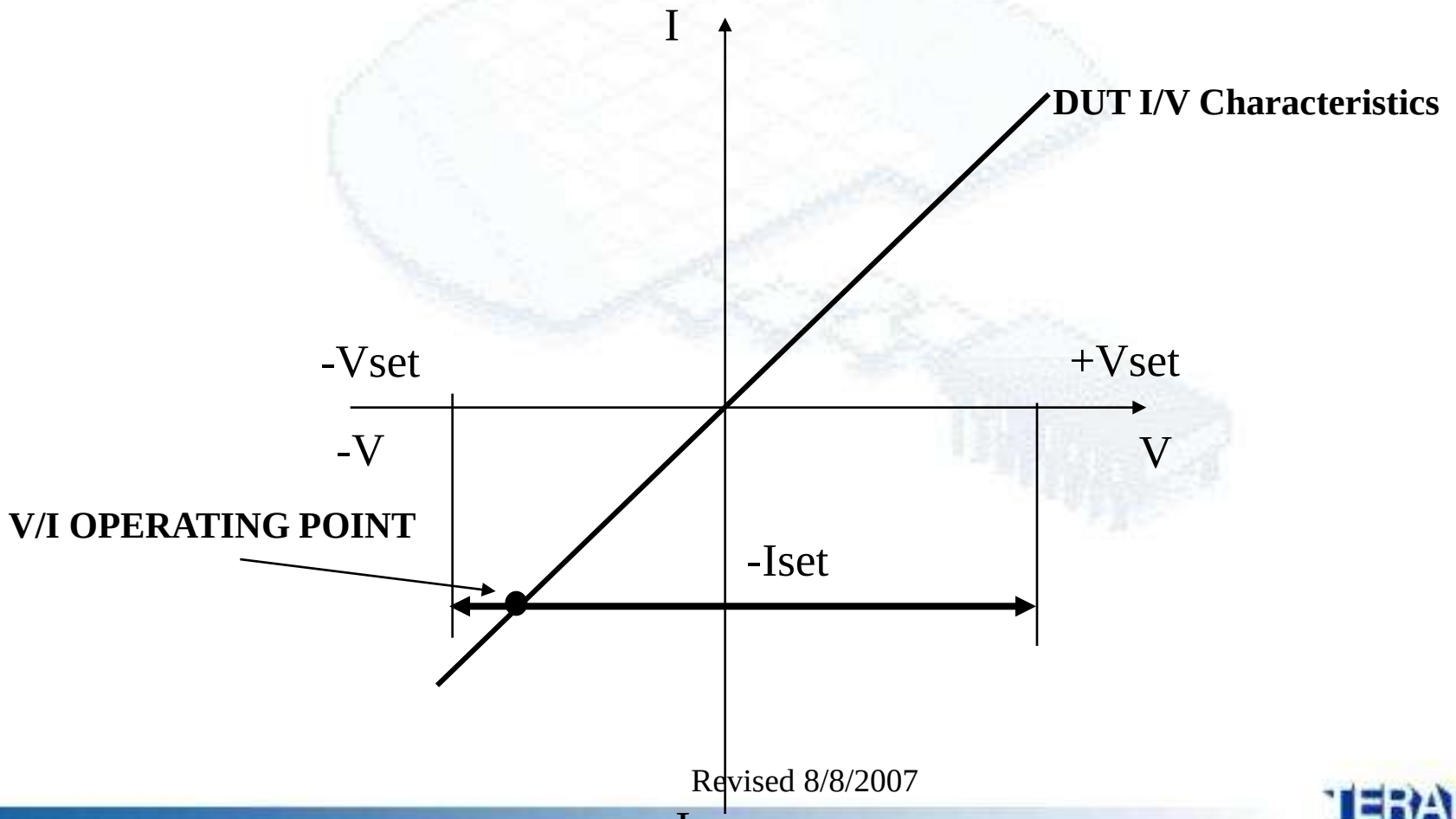
VOLTAGE/CURRENT (VI) SOURCE

The Current Source: The operating point in force I mode.



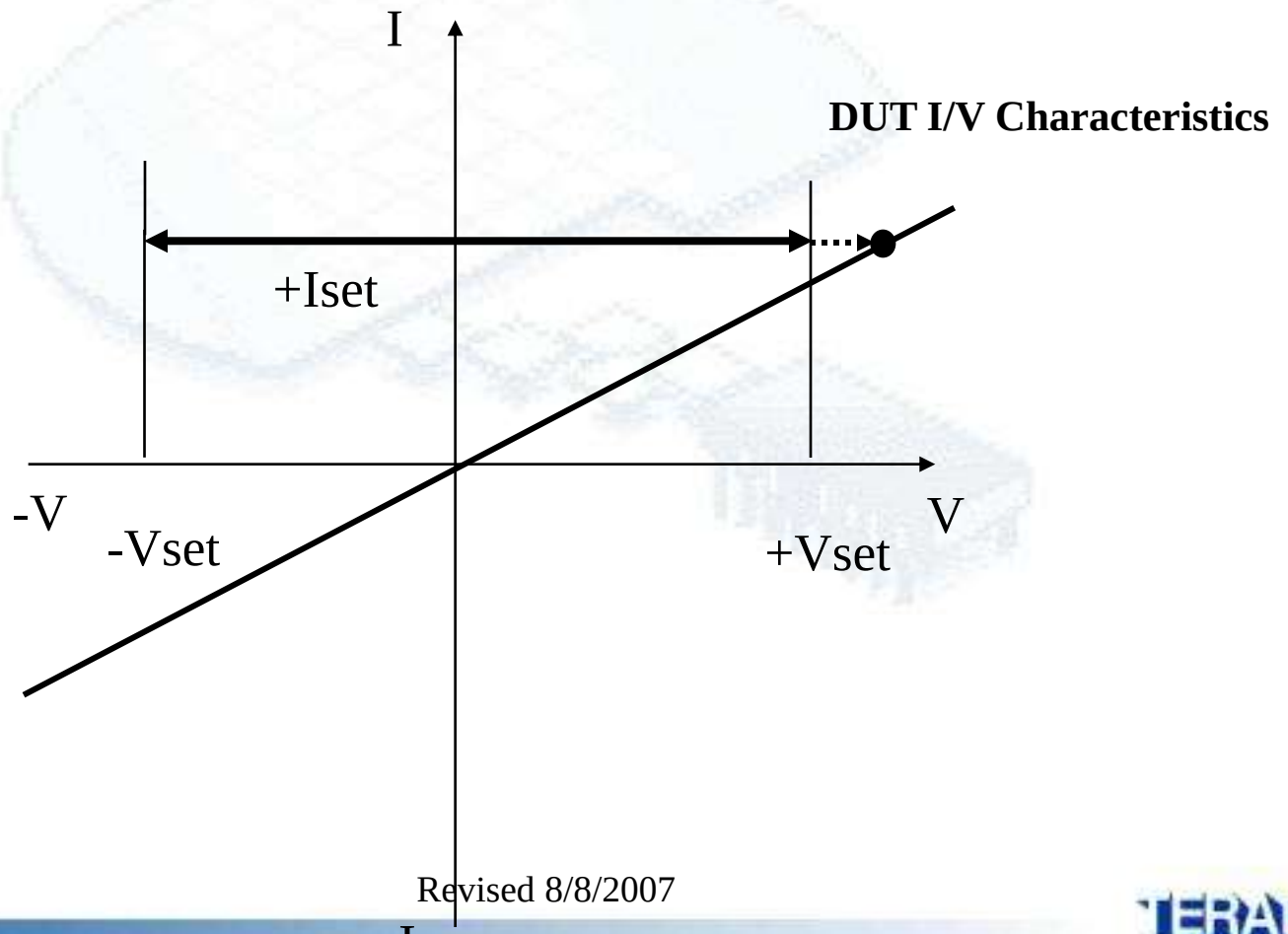
VOLTAGE/CURRENT (VI) SOURCE

The Current Source: Opposite polarity current forcing mode is supported by the VI source. Current flowing into the source is called sink current.



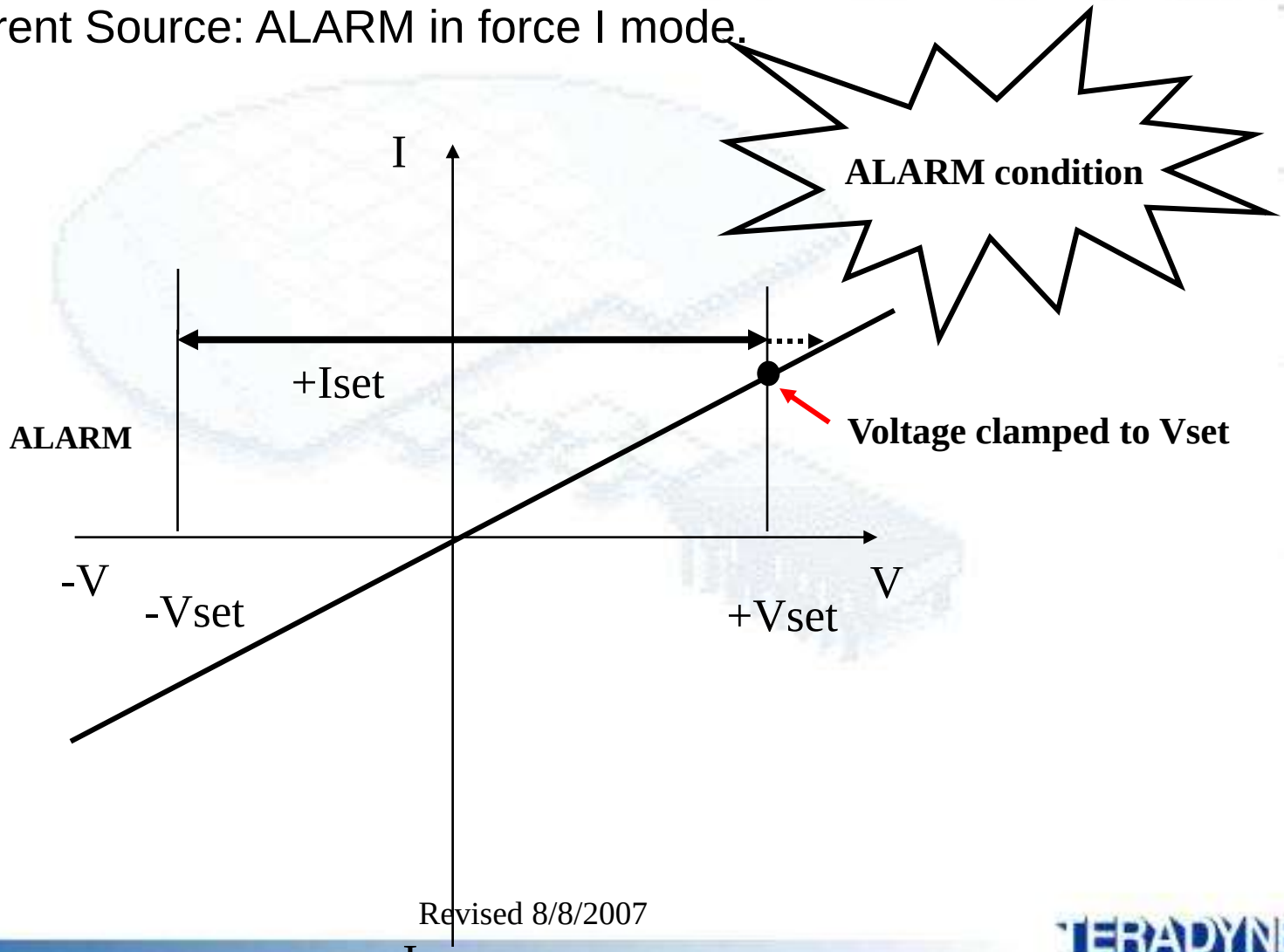
VOLTAGE/CURRENT (VI) SOURCE

The Current Source: What happens when, in force I mode, the operating point is above Vset?



VOLTAGE/CURRENT (VI) SOURCE

The Current Source: ALARM in force I mode.



PMU – Parametric Measurement Unit

Some ATE system have a System PMU which allows connection to other instruments within the system for the purpose of DC measurement (current/voltage measurement).

The PMU can operate in either Force-Current-Measure-Voltage or Force-Voltage-Measure-Current modes.

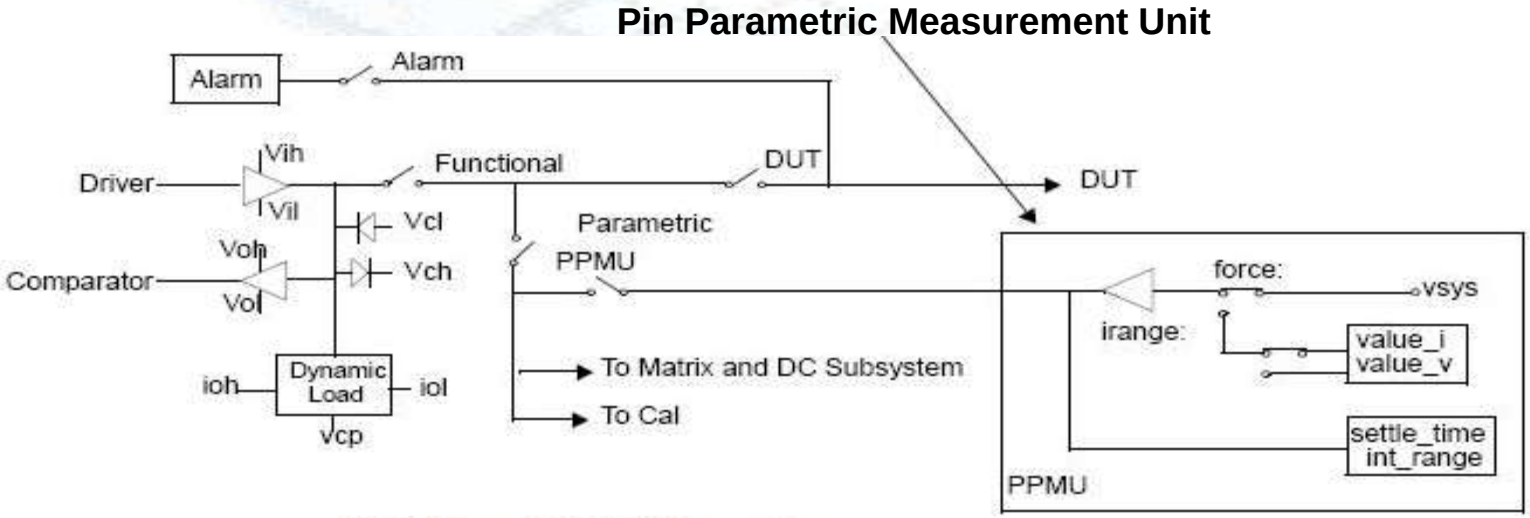
This enables a DC measurement to be performed on your device pins even if these pins are physically assigned to Digital Pin Electronics or other Analog instruments.

In addition to this system PMU, some ATE have built-in individual ‘PMU’ on each of their Digital Pin Electronics Channel (called PPMU – Pin Parametric Measurement Unit). In such case, typically the System PMU would have better current/voltage ranges, while the PPMU has lesser current/voltage capabilities.

PPMU – Pin Parametric Measurement Unit

Today PPMU is a common feature in most ATE, that some newer ATE even comes without the System PMU.

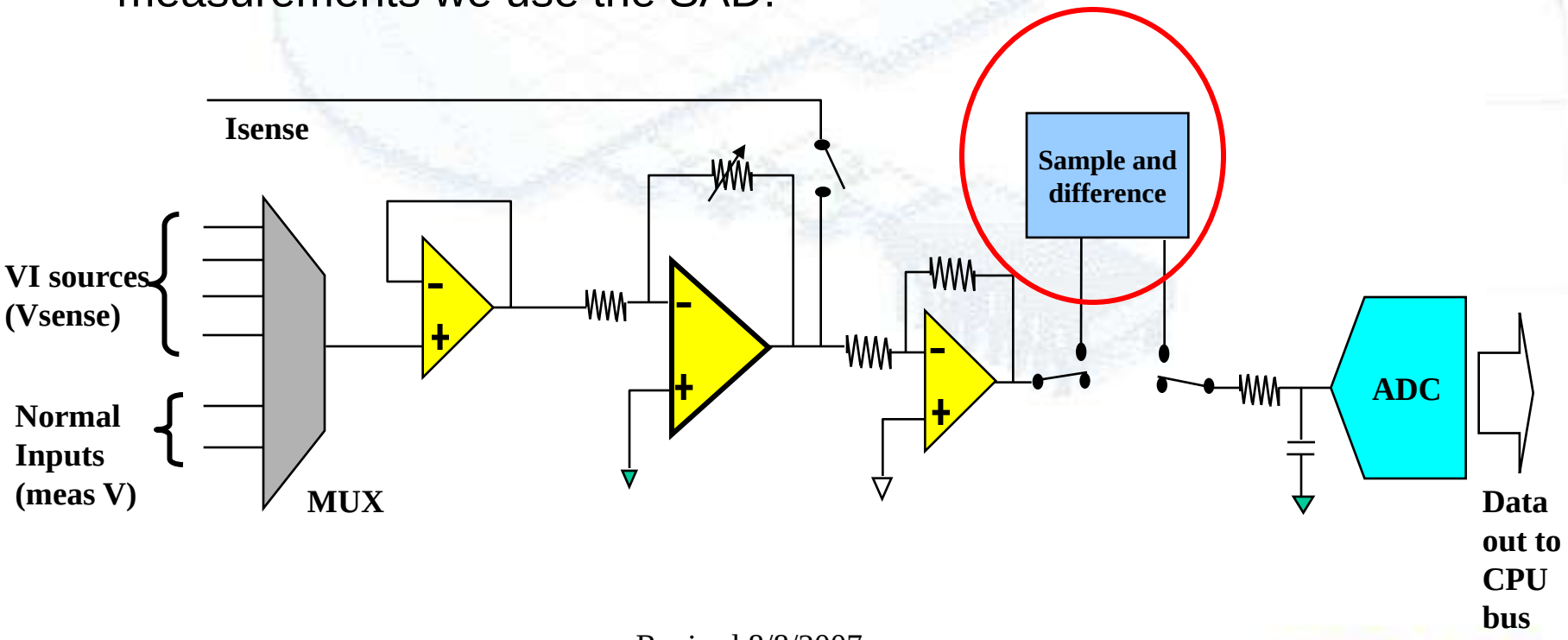
The availability of PPMU enables DC measurement to be done in parallel for each of this Digital Channel if needed. This PPMU is now commonly used for performing tests such as Continuity and Leakage.



PPMU on a Digital Channel

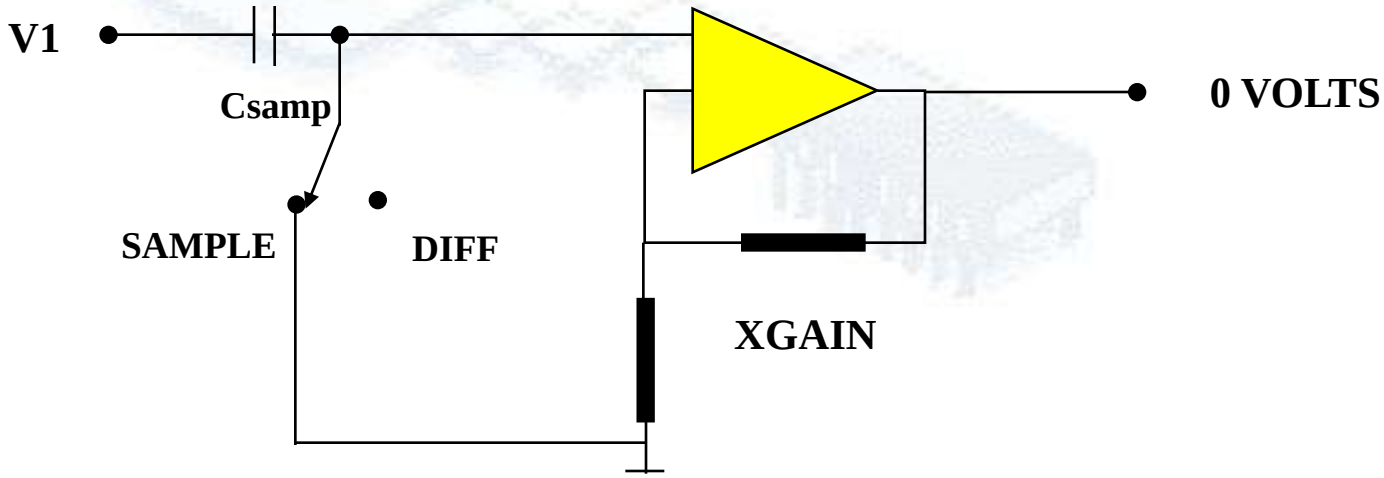
DC METER

The Sample and Difference part measures delta voltages that are very close. If an attempt is made to get the difference between 2 measured voltages at 5.000v and 5.001v in the 20V range, we cannot get better than the resolution of 2.5mV! For this type of measurements we use the SAD:



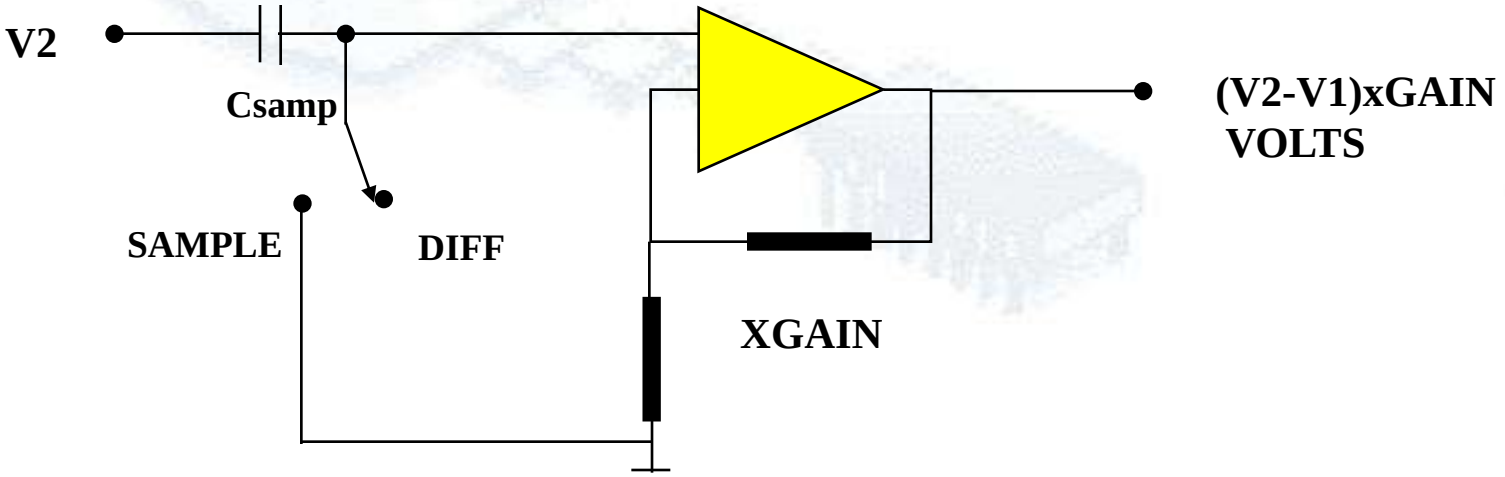
DC METER

The structure of the SAD is shown below. The Csamp
Samples the first voltage from the dut, V1.The SAD output is at 0V since
The OpAmp's input is grounded to charge up Csamp:



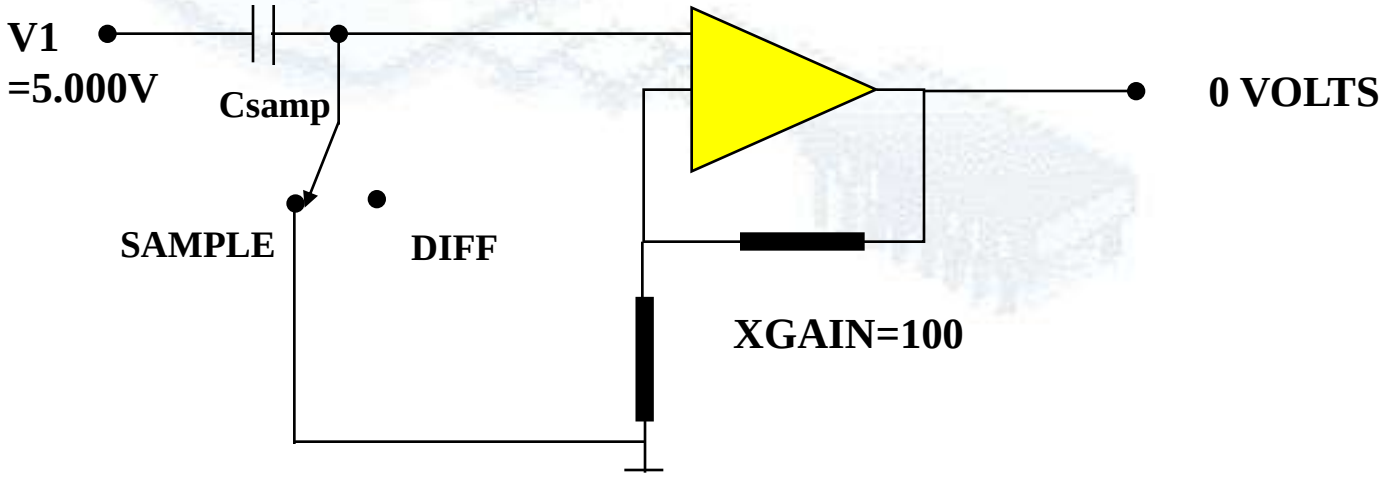
DC METER

The SAD is switched to DIFF mode and then V2 is applied at The input.This subtracts from the stored voltage in Csamp to a resultant of V2-V1:



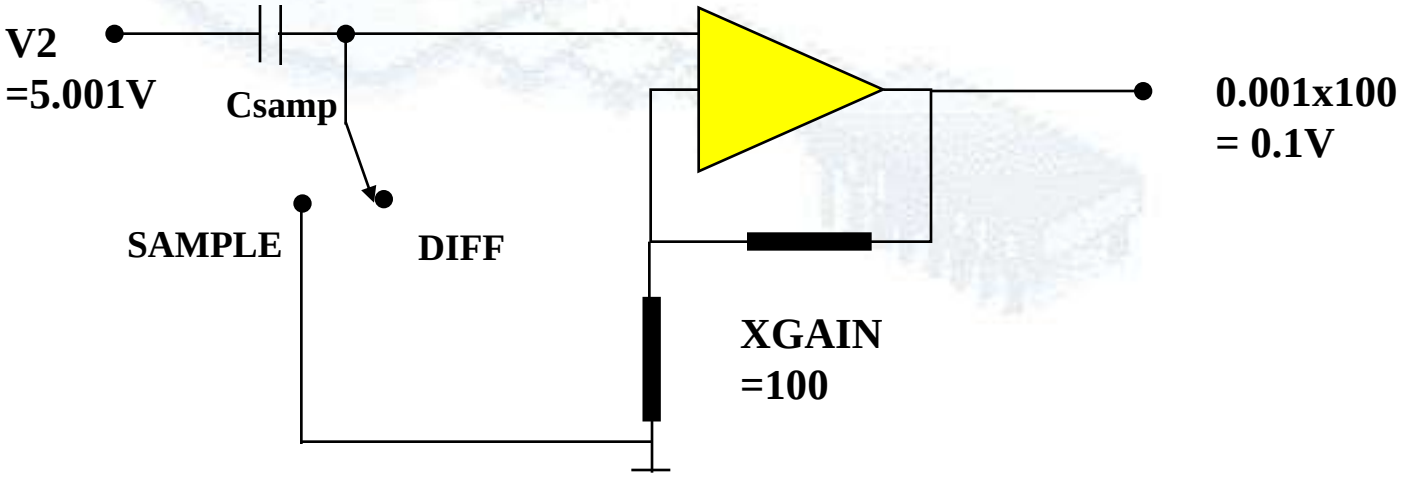
DC METER

Consider now using this circuit to measure the difference of the 5.000V and 5.001V mentioned earlier:



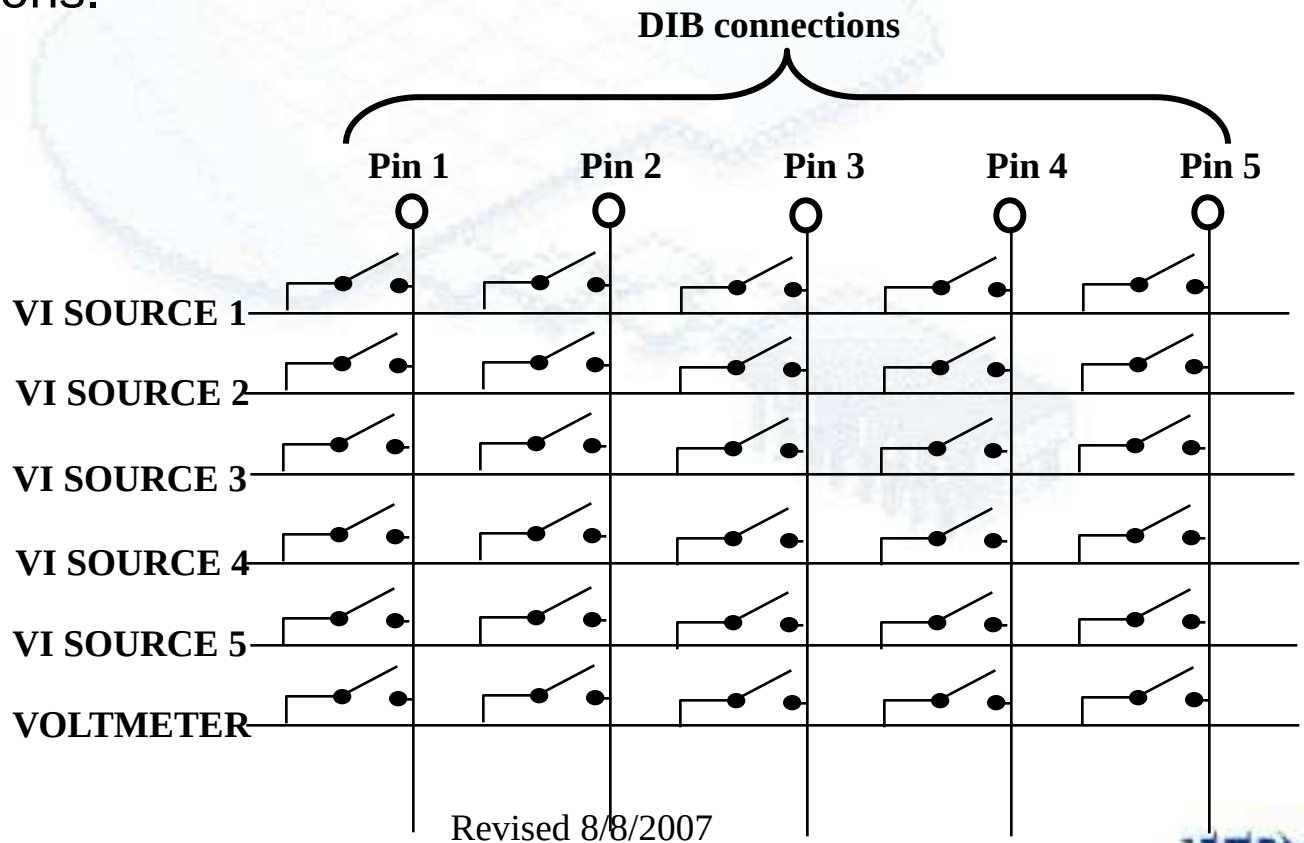
DC METER

The output is gained X100 and goes to the +/-10.24V ADC.
The resolution of measurement now is 1.25mV/100 = 12.5uV which is much more acceptable for a 1mV difference.:



DC MATRIX

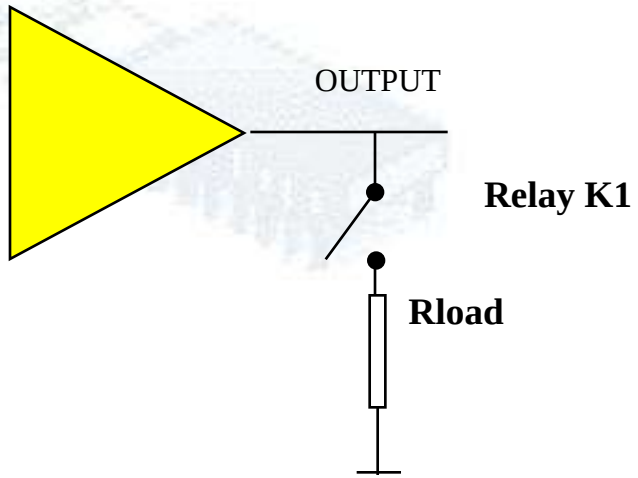
Here is a general purpose 5X6 matrix. Every instrument can be connected to any pin which hardwire to the Device Interface Board (DIB). Each relay and line actually represent the Force,Sense and Guard connections.



RELAYS AND RELAY CONTROL BIT

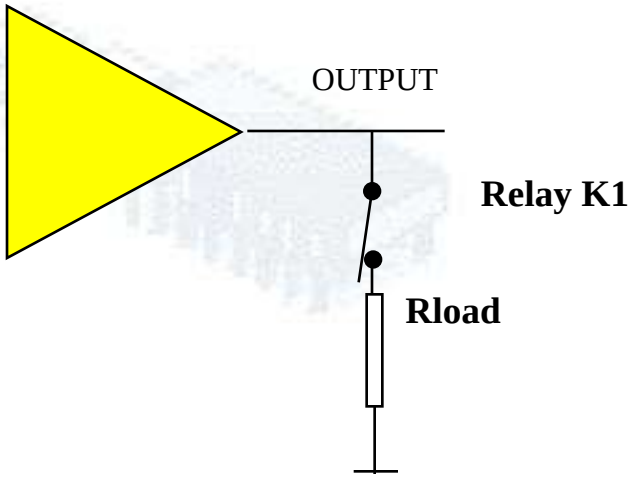
It is often necessary to configure the DUT differently for different tests.This is typically achieved by mechanical relays.

Relay K1 used to connect/disconnect Rload: OFF



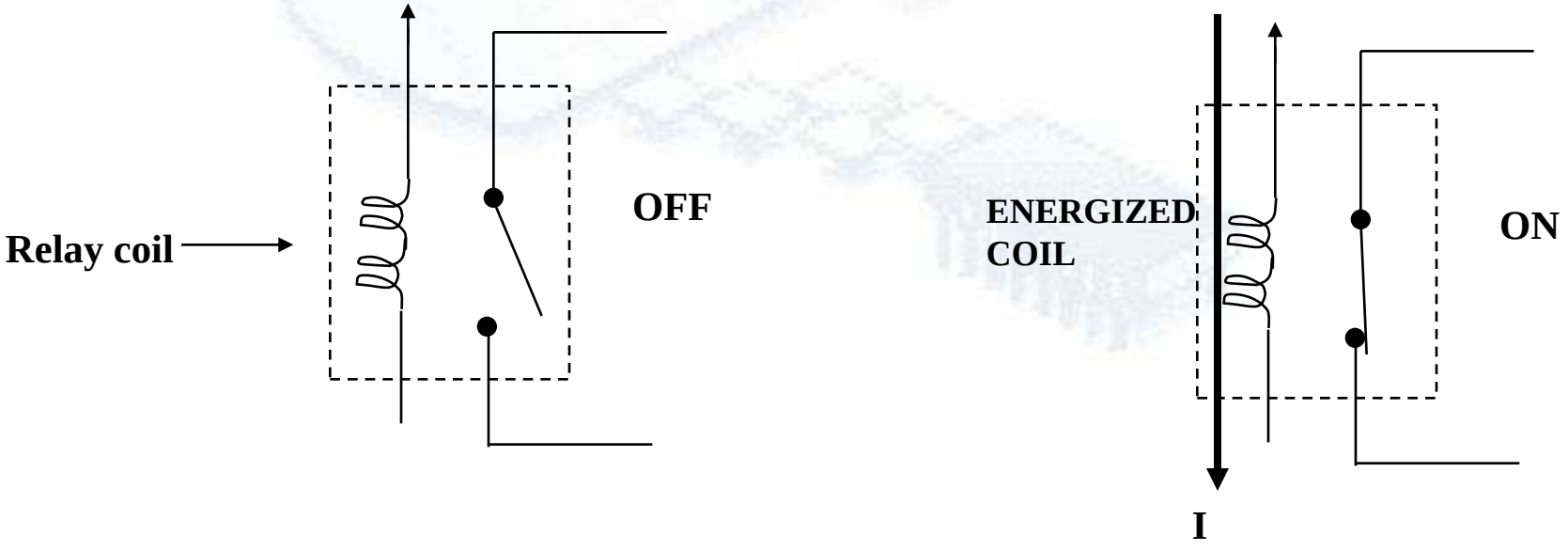
RELAYS AND RELAY CONTROL BIT

Relay K1 used to connect/disconnect Rload: ON



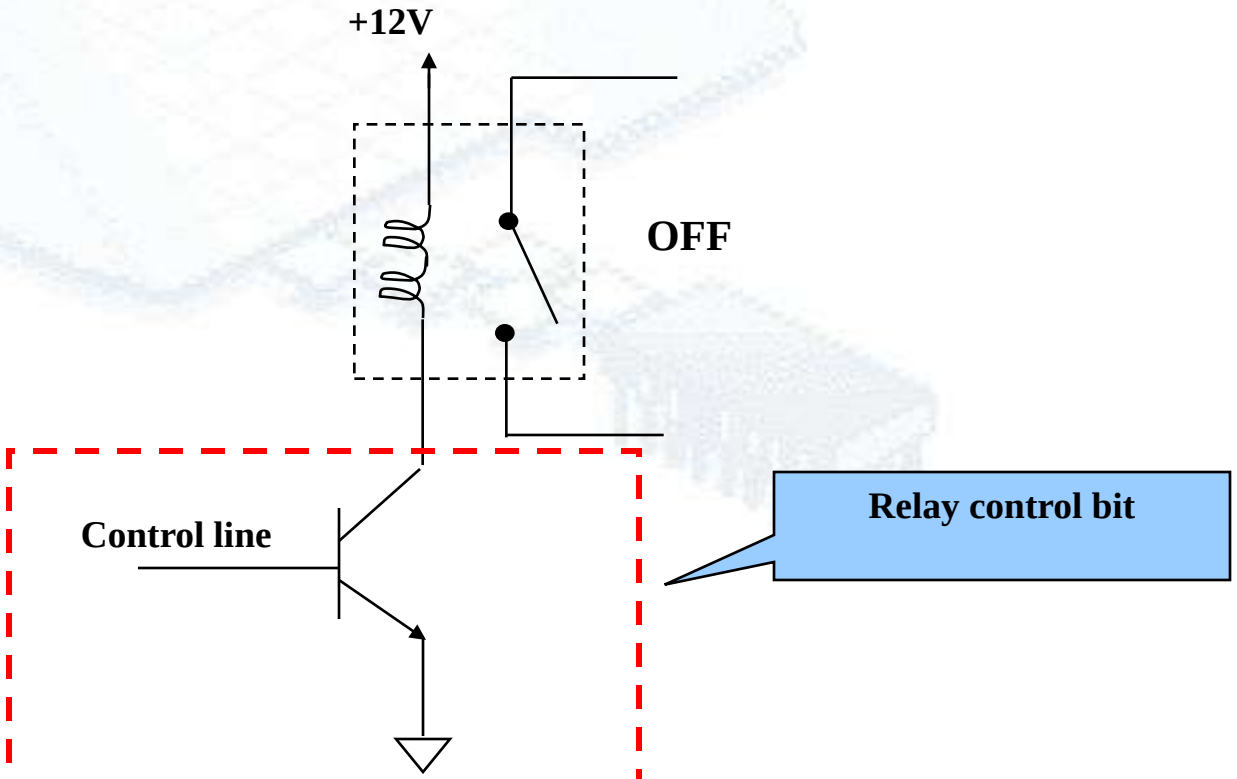
RELAYS AND RELAY CONTROL BIT

The mechanical relay consists of a coil and a switch. The coil need to be energized for the switch to throw. The coil is energized by a current flow at the level of the relay's specification.



RELAYS AND RELAY CONTROL BIT

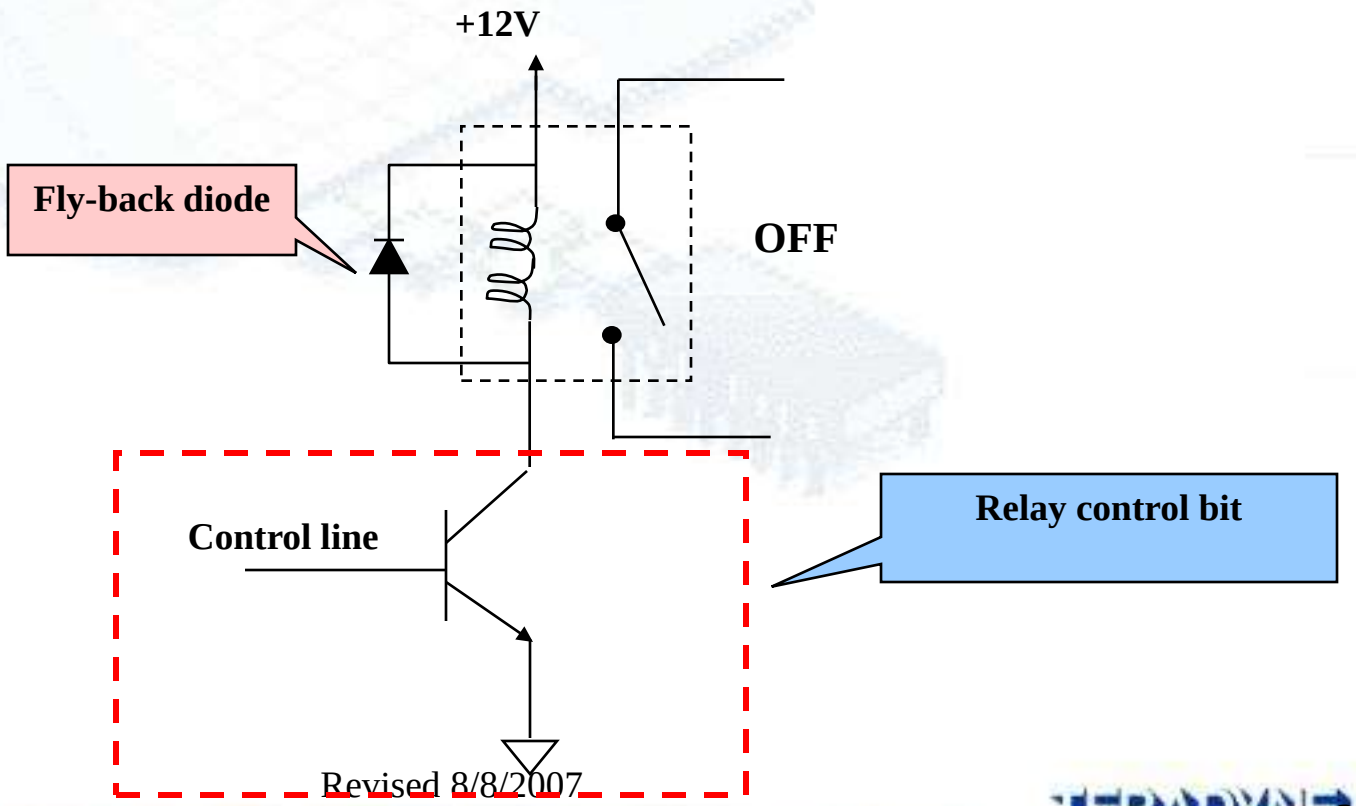
Most ATE have multiple relay control bits that work to energize and de-energize relays' coils.



Revised 8/8/2007

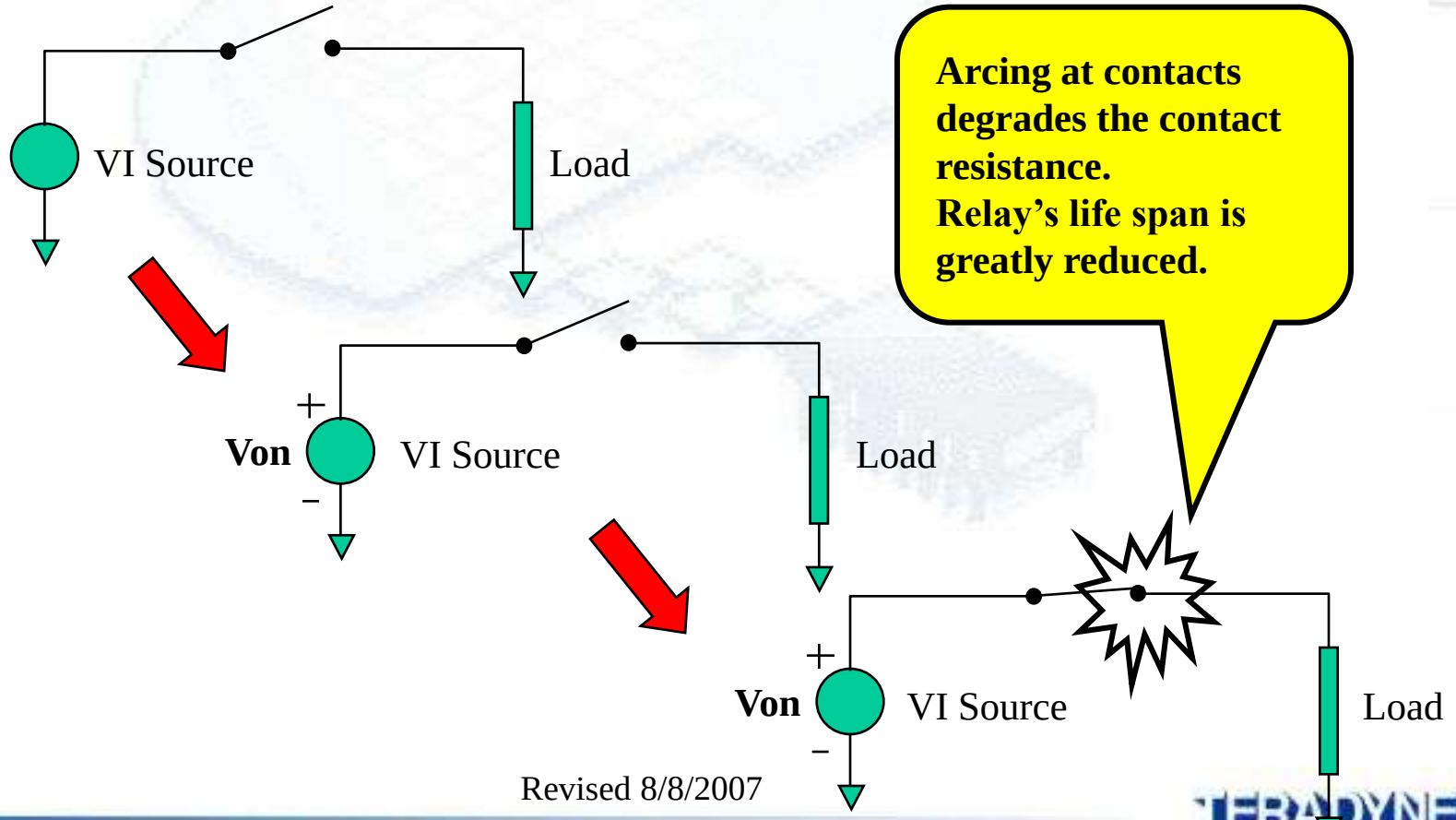
RELAYS AND RELAY CONTROL BIT

A diode is typically connected across the relay coil to minimize the effects of “kick-back” voltage or back emf when the current through the coil rises and falls rapidly. This back emf will try to sustain the current.



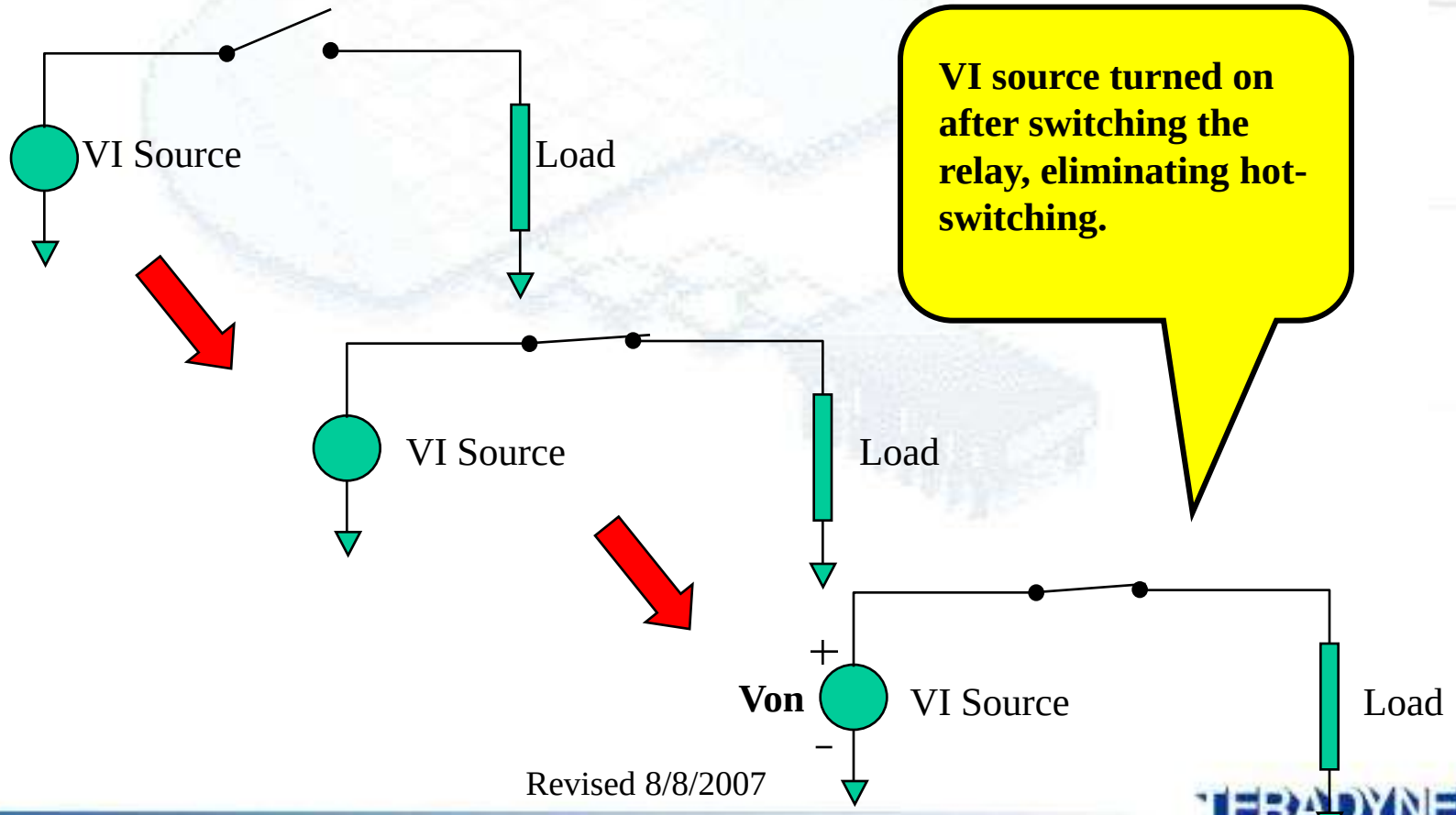
HOT-SWITCHING !!

THE FOLLOWING SEQUENCE ILLUSTRATES HOT-SWITCHING OF RELAYS.



HOT-SWITCHING !!

THE FOLLOWING SEQUENCE ELIMINATES HOT-SWITCHING.



Self-Assess Questions

1. Which of the following tests you cannot perform with a PMU only?
   VOL, VOH, IIL, IOZL, IIH, IOL, VIH

2. Which of this is a common Force-Current-Measure-Voltage Test?
   Continuity, Leakage, IDD, VOL, IOZH

3. Let say you use a VI Source in Force Voltage mode, and Alarm is encountered due to preset clamp being violated. What is exceeding the allowed limit (clamp), voltage or current?

4. For a VI Source, typically you have a Force, Sense and Guard line. The Force and Sense line meet at a point as close to the DUT as possible. What is the main difference between Force and Sense line?

5. For Continuity test, the pin under test is forced a small current and the resultant voltage is measured. What do you do with the rest of the device pins during this?

DIGITAL FUNCTIONAL TEST

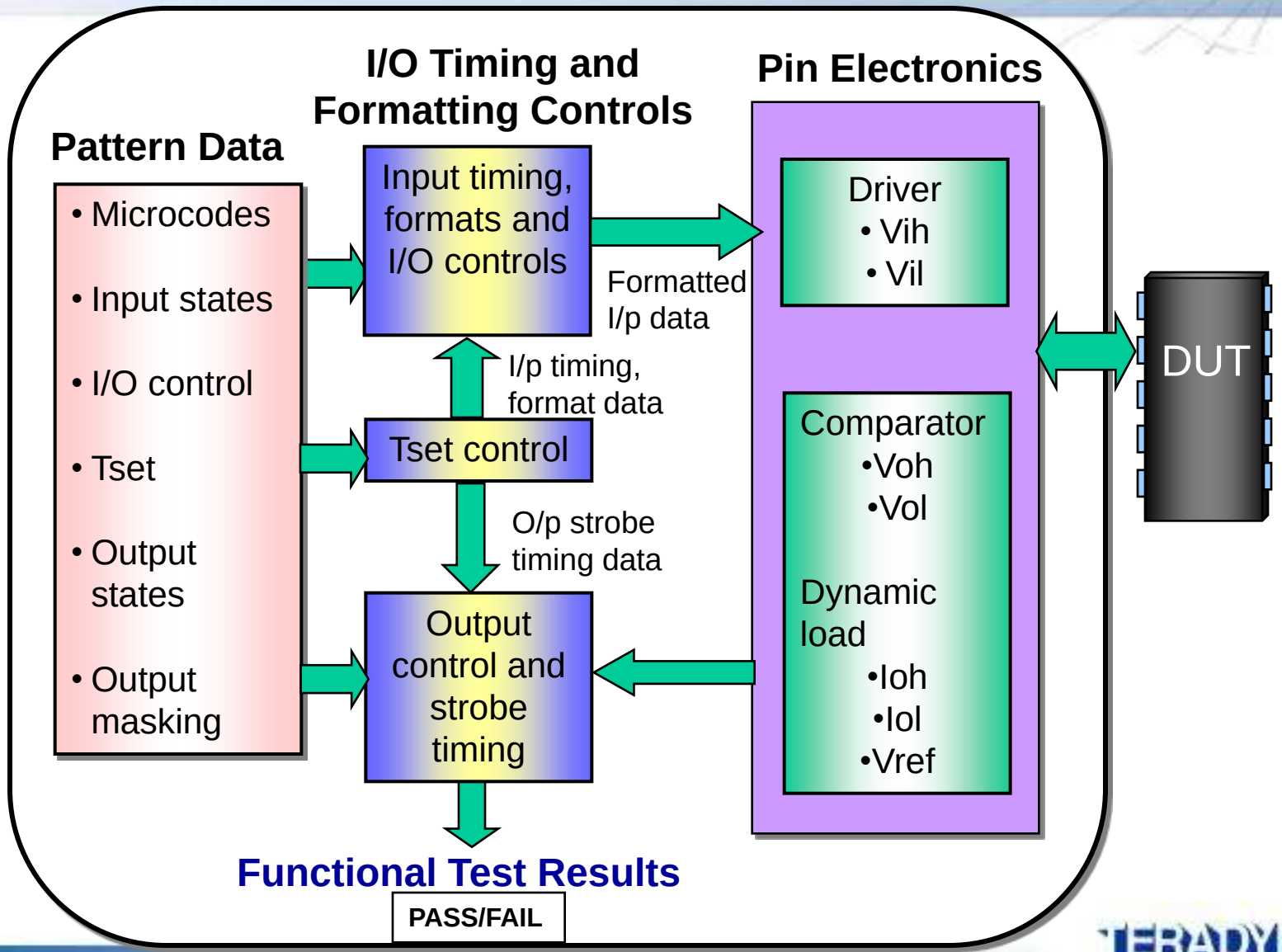
Introduction

- To verify that the DUT will correctly perform its intended logical functions, test vectors or truth tables must be created which can detect faults within the DUT.
- The ability of truth table to detect faults can be measured and is referred to as fault coverage.
- The test pattern (test vectors) combined with test timing, levels and loading currents is called as a functional test.

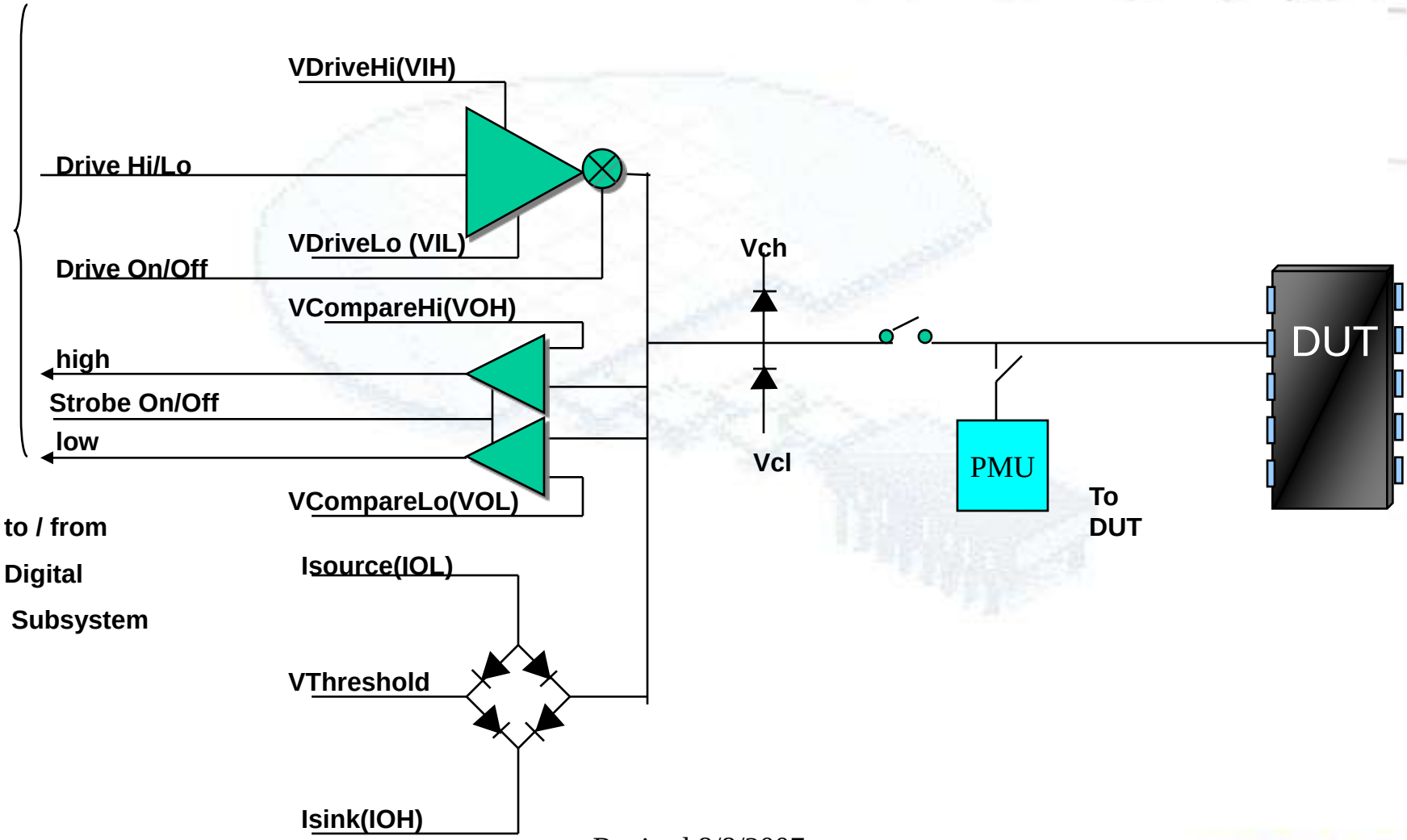
Input = Test Vector + Levels + Test timing + Signal Format.

Output = Test Vector + Levels + Output Test timing

Functional Testing Block Diagram



Pin Electronics



Pin Electronics

Pin Electronics is otherwise called as Channel card .

- It is the interface between the digital subsystem and the DUT.
- It contains the following circuitries
  - Drivers to drive the inputs to the device.
  - Switching circuits to the drivers On and OFF
  - Comparators to detect and compare the output levels
  - Programmable current loads to act as a load to the DUT outputs
  - Used as a connection point to a PMU

Test Concepts

Digital Functional Test

- The signal definition of a digital test needs to define all of the parameters required to generate the stimulus and response required by the DUT.

- This means more than just defining the sequence of logic-1's and logic-0's necessary to test a digital DUT. It is also necessary to include detailed timing and voltage level information.

Test Concepts

A Functional Test consists of below:

1. Pattern

Vectors that contain the drive and compare data

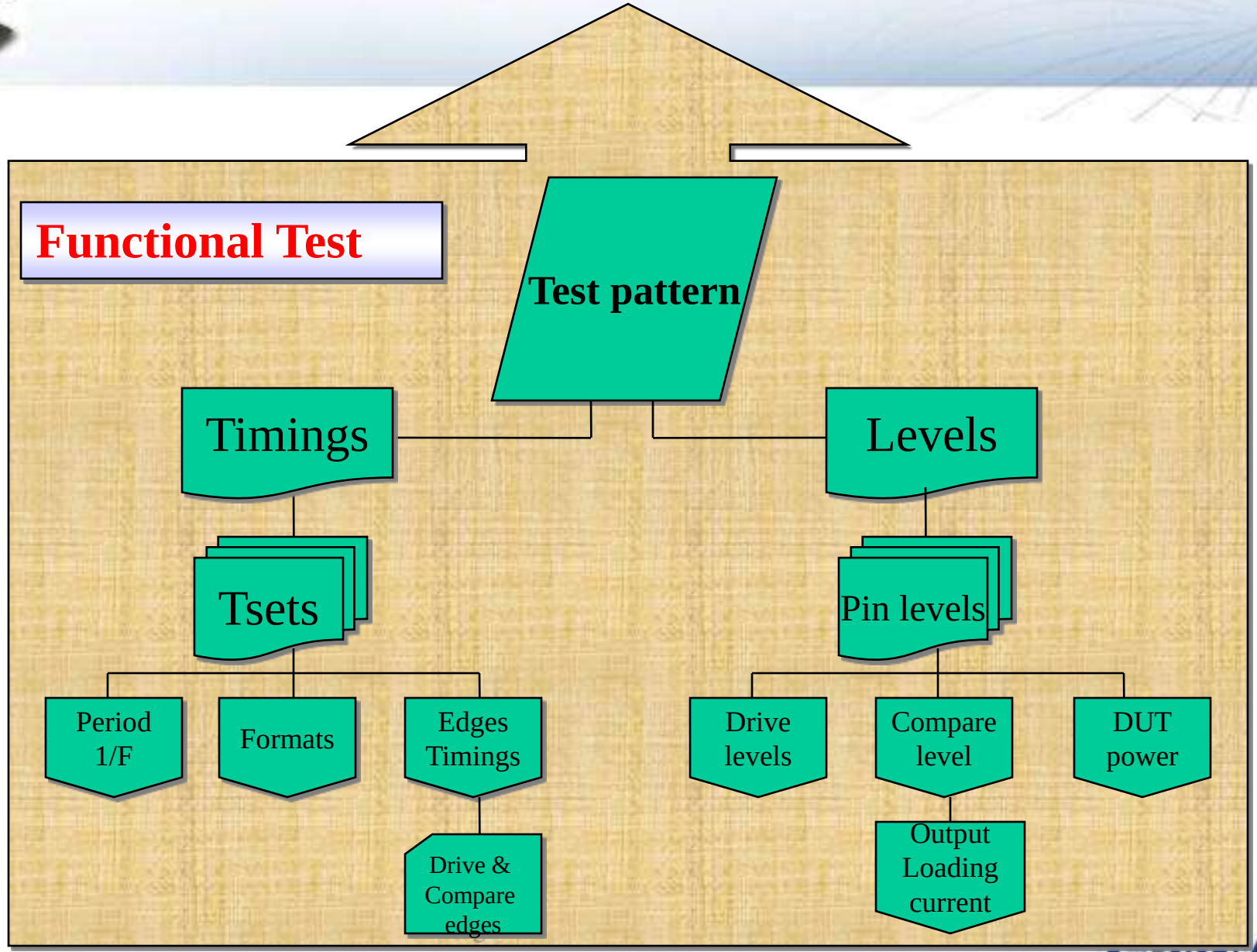
2. Timing

Timesets with Edgesets to provide format, drive and compare edge timing

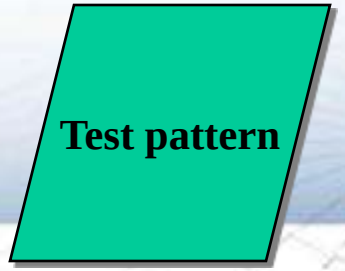
3. Levels

For signal pin drive and compare levels, and for the device power pin

Test Concepts



Test Concepts



Patterns

- The patterns contain the logic values that are required to test the DUT.
- The pattern data must be combined with the timing information to create the correct stimulus and measure the correct response at the DUT .
- Each logic state needs to be able to indicate if the logic applies to stimulus or response.
- The pattern values need to include not only logic 1 and 0 data but also High(H), Low(L), Tri-state(Z) and “don’t care” (X) for outputs.

Test Concepts

Timings

Timings

- Pattern supplies a list of logic to be driven-to, or compared-from the DUT.
- The timing information indicates when these happen (Drive/Compare)
- The digital functional test data must explicitly state WHEN every edge should occur.
- Timesets (Tsets) will have the details of the period (cycle).
- Edgesets (Esets) will indicate format and the timing details of the edge placements for the drive and compare data .

Test Concepts

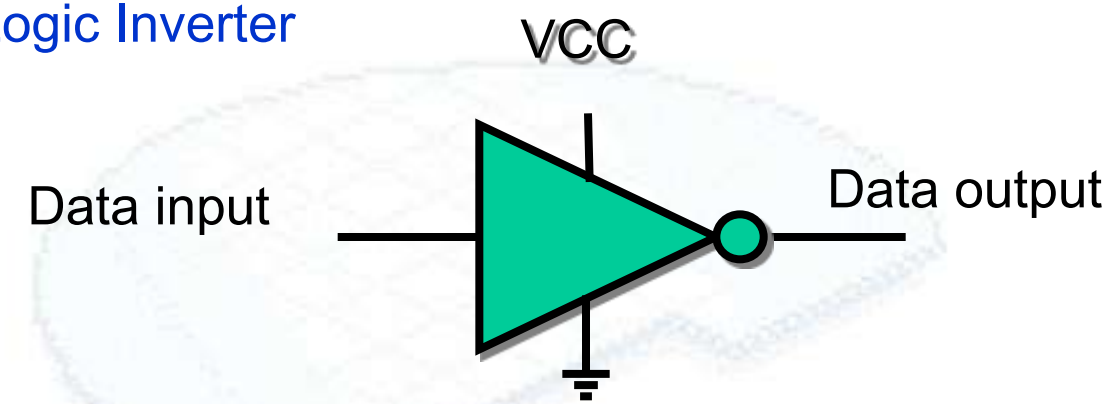
levels

Levels

- The third parameter is the voltage and the currents values assigned to the logic values in the pattern data .
- These levels may be different for different pins on the DUT.
- Levels include the input voltages for the Logic inputs data (Login 1 & Logic 0) in the pattern and the output levels (Logic H & Logic L) and the thresholds response data.

Test Concepts

Example of Logic Inverter

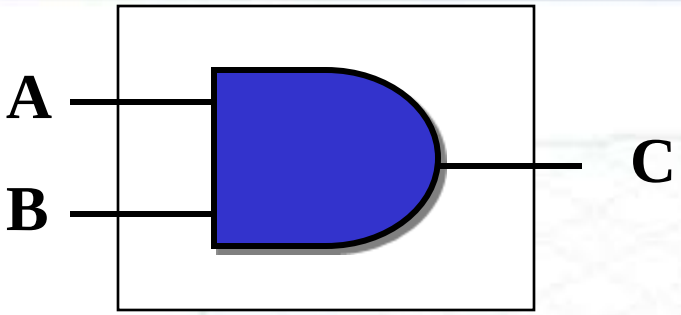


- Input data is defined as a 1 or 0
- Output data is defined as an H or L

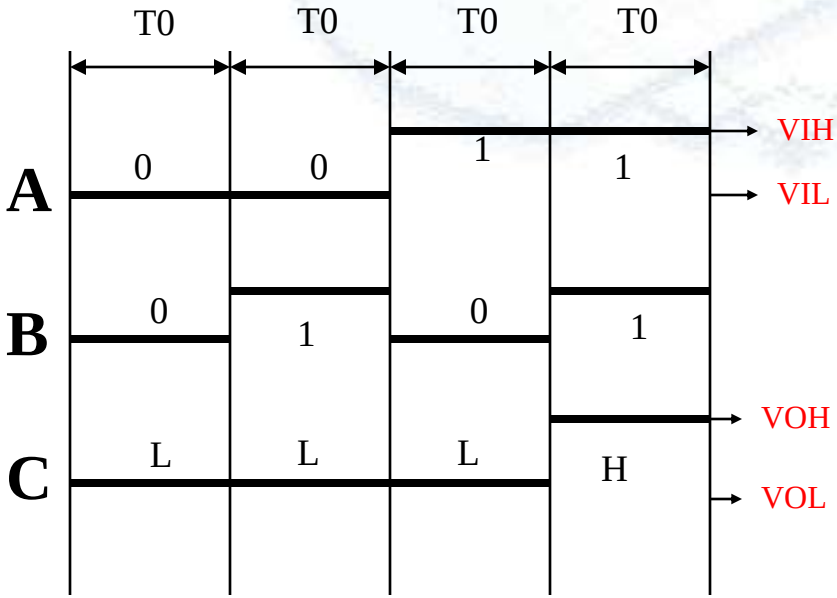
TRUTH TABLE

Input	Output
1	L
0	H

Functional Truth Table



AND Gate



Timing Diagram

Truth Table

Input	Input	Output
A	B	C
0	0	L
0	1	L
1	0	L
1	1	H

Timing Format = NRZ

Test Concepts

Defining the Operation of a DUT with a Truth Table

Example: AND GATE

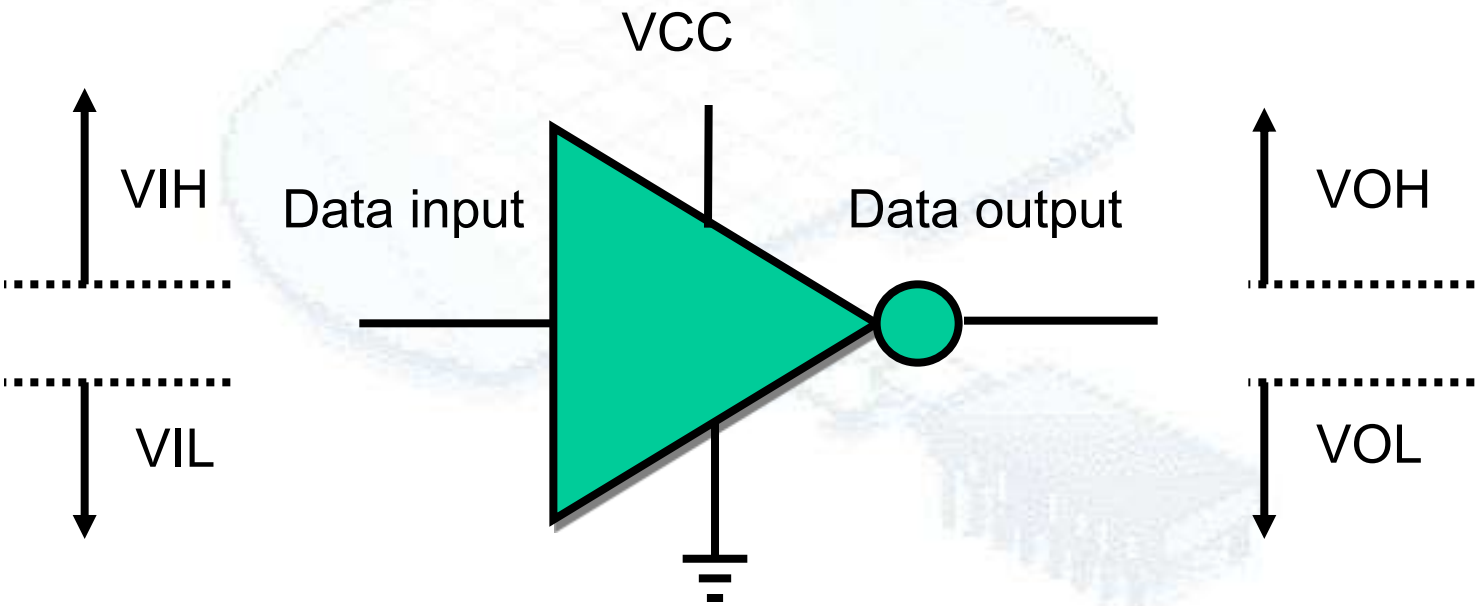
	IN1	IN2	OUTPUT
Vector 1	0	0	L
Vector 2	0	1	L
Vector 3	1	0	L
Vector 4	1	1	H

Where

- The 1s and 0s are the data.
- A line of 1s and 0s is called a vector.
- The vectors and, therefore, the data are part of what is called the pattern.

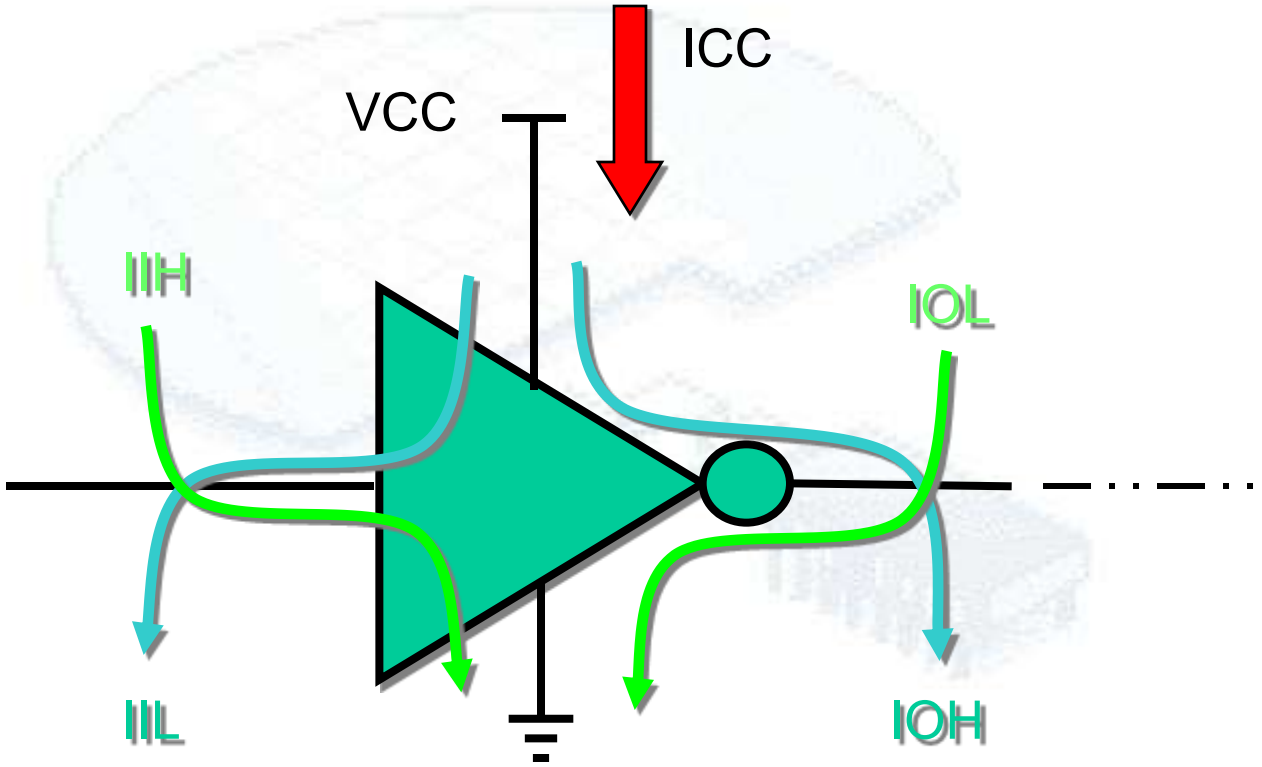
Test Concepts

Definitions : Voltages



Test Concepts

Definitions: Currents



ICC is supply current.

Important Parameters

Important Parameters check during a functional test

- VDD Min/Max :DUT Power Levels
- VIL/VIH :Input Levels
- VOL/VOH :Output Levels
- IOL/IOH :Output Current Loading

- Test Frequency :Cycle Time Used For Test
- Input Vector :Wave Shape Of Input Signal
- Vector Sequencer :Start Or Stop Point Of Signal

Important Parameters

- Input Signal Timings :

  Clocks / Setups /Holds / Controls

- Output Signal Timings:

  Output strobe - When Will Output Sampled

Test Concepts

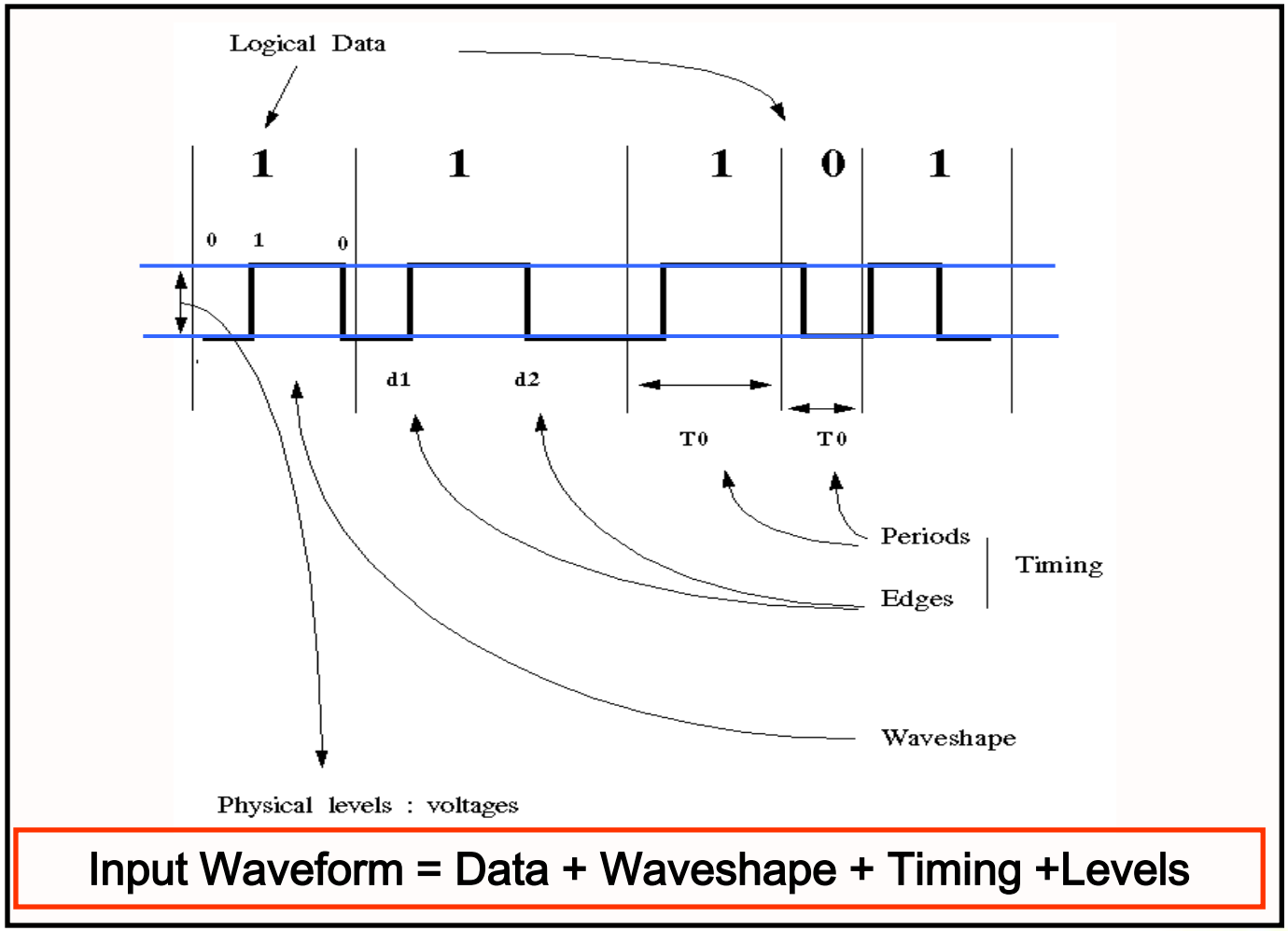
What is Digital Functional Testing?

Digital Functional Testing is to:

1. Define input waveforms per DUT requirements; and
2. Check output waveforms against expected data of DUT

Test Concepts

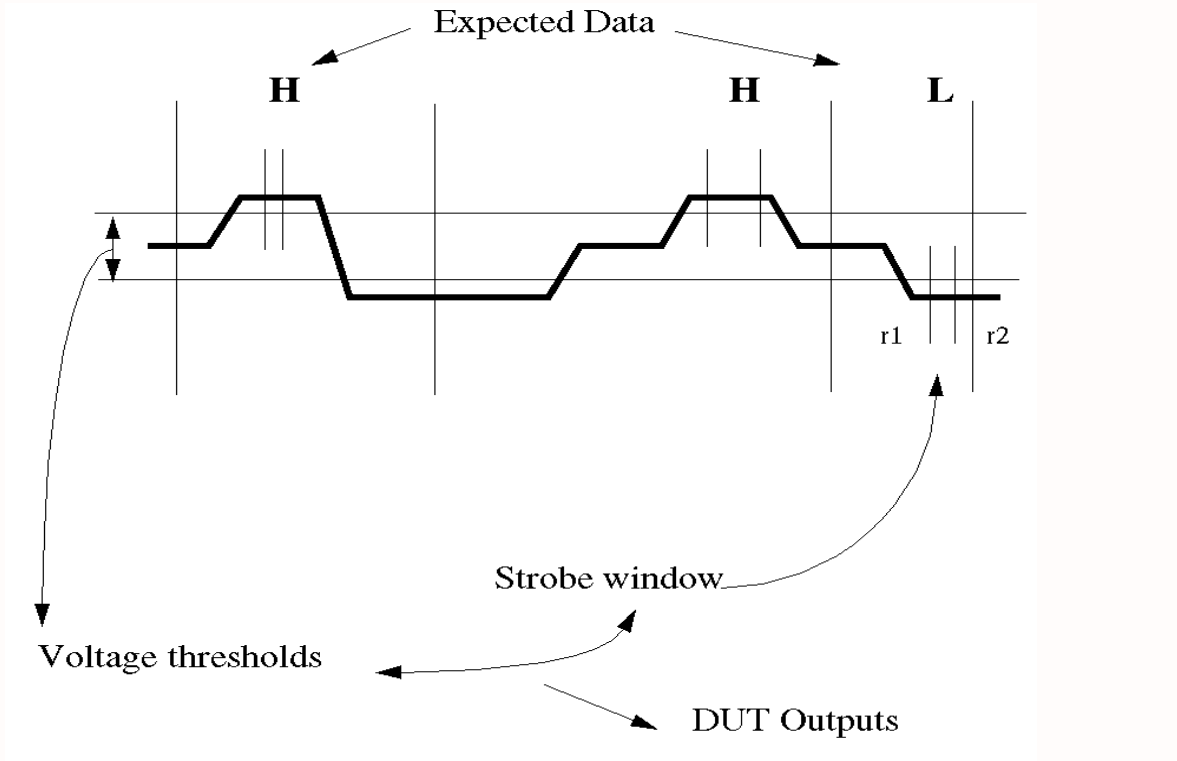
Input Waveform



Input Waveform = Data + Waveshape + Timing +Levels

Test Concepts

Output Waveform



Output Waveform = Data + Timing + Levels

Input signal

Input signal waveform is created by

- Test Vector Data (Logic Data to DUT)
- Input Signal Timing (Edge Placement Points)
- Input Wave Shapes (Signal Format)
- Input Voltage Levels (VIH/VIL)
- Time Set Selection (Vector Frequency)

Signal Formats

- Signal formats,when combined with vector data,edge placements and input levels,define the wave shape of input signals to the DUT.
- Signal format is used to generate proper signal that required to correctly control any digital logic circuit.

Types of Signal Formats

- NRZ : Non Return to Zero
- RZ : Return to Zero
- RO : Return to One
- SBC : Surround by Compliment

Timing *Edges*

•These are signal timings to control drive and compare circuit of the Pin Electronics

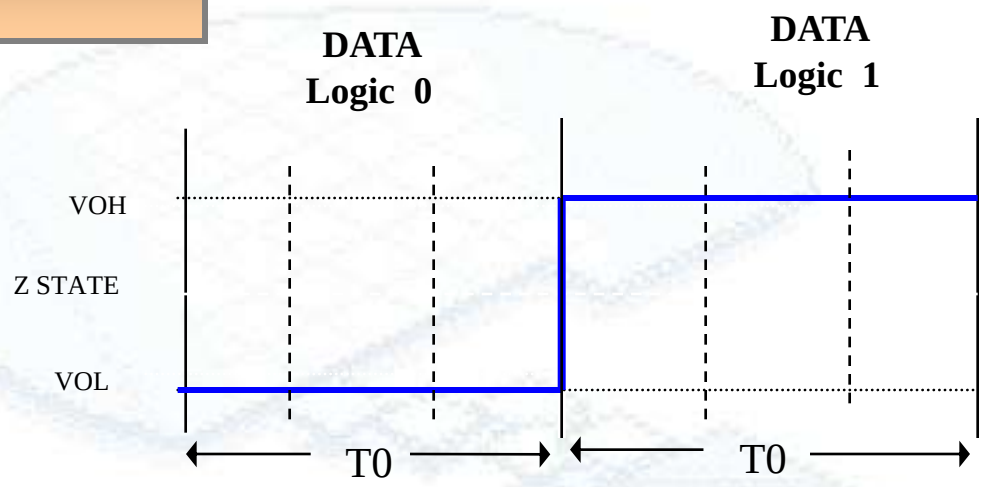
- D0 or Drive On - *Start of cycle for each channel*
- D1 or Drive Data - *Start of drive pulse for each channel*
- D2 or Drive Return - *End of drive pulse for each channel*
- D3 or Drive Off - *Time of I/O switch*

- R0 or Compare Start (On)
  - *Start of compare window for each channel (window strobe)*

- R1 or Compare End (Off)
  - *End of compare window for each channel (window strobe) or edge strobe*

Types of Signal Formats

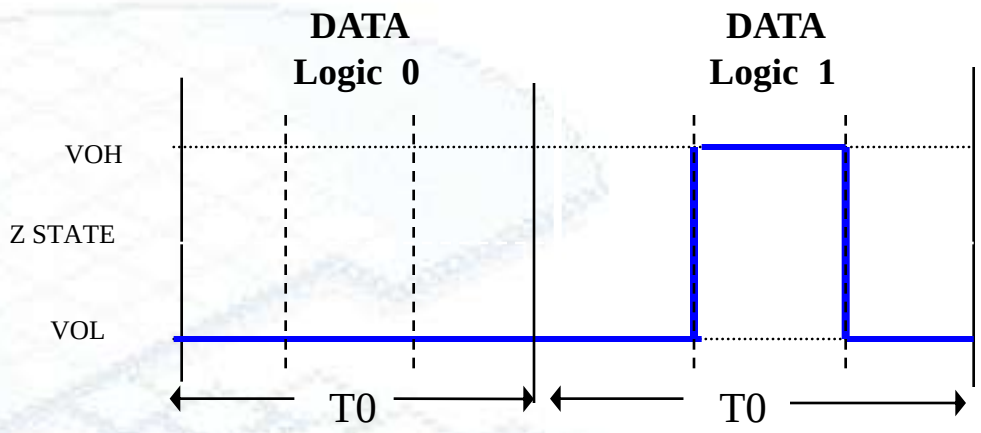
Non Return to Zero



- NRZ represents the actual data stored in vector memory and contains no edge timing.
- NRZ data changes only at the beginning of each cycle.

Types of Signal Formats

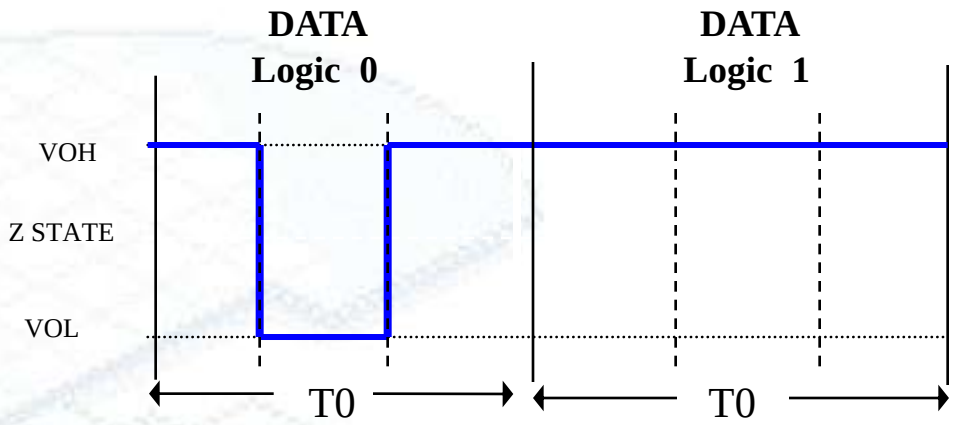
Return to Zero



- RZ provides a positive pulse when vector data is logic1 and no pulse when vector data is logic 0.
- This signal format can provide a positive clock when all vector data for the pin is logic 1.

Types of Signal Formats

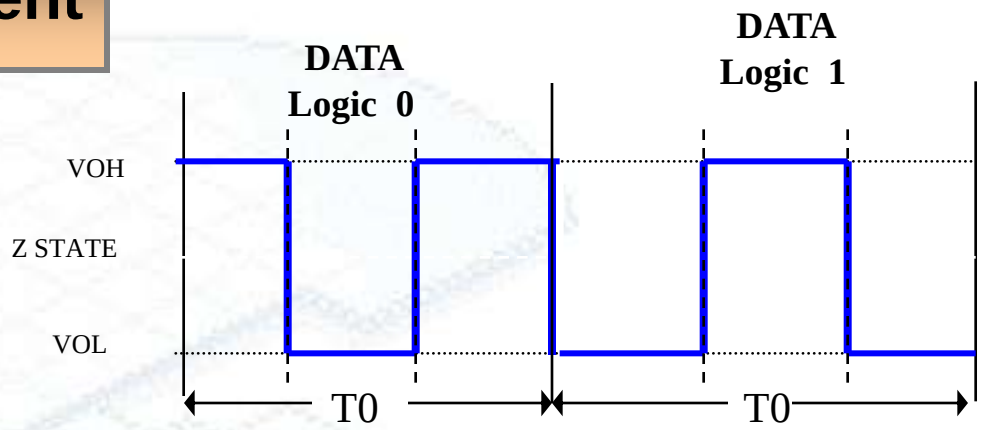
Return to One



- RO provides a negative pulse when vector data is logic 0 and no pulse when vector data is logic 1(the signal remain in logic1).
- This format can provide a negative clock when all vector data for the pin is logic 0.

Types of Signal Formats

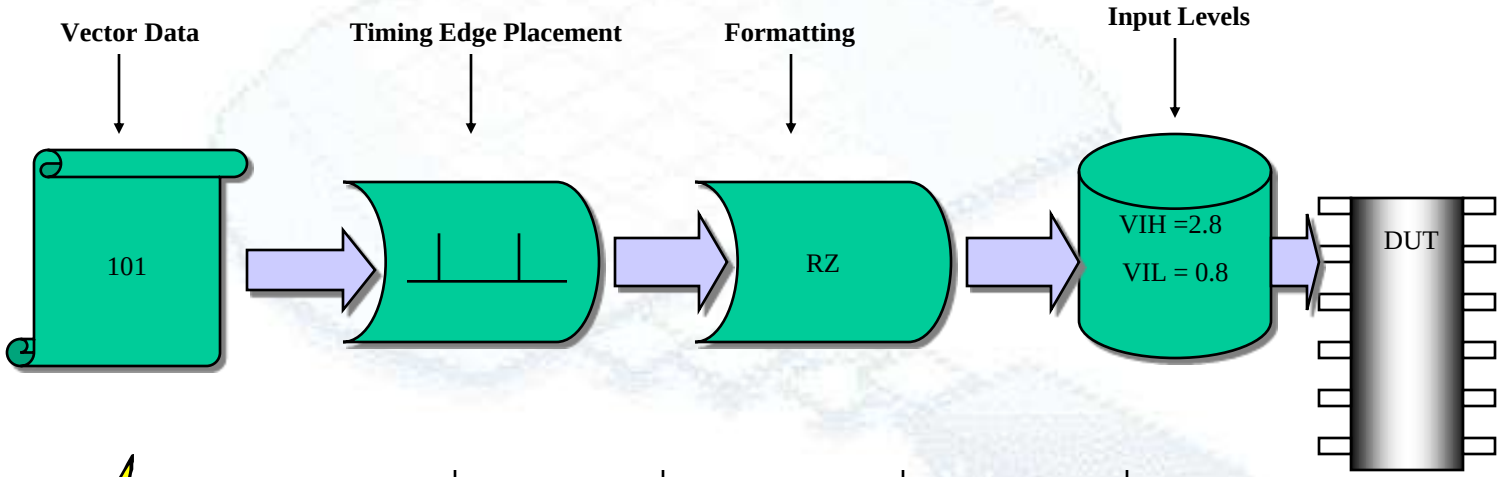
Surround By Compliment

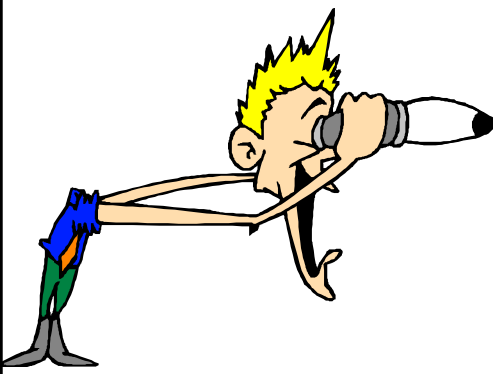


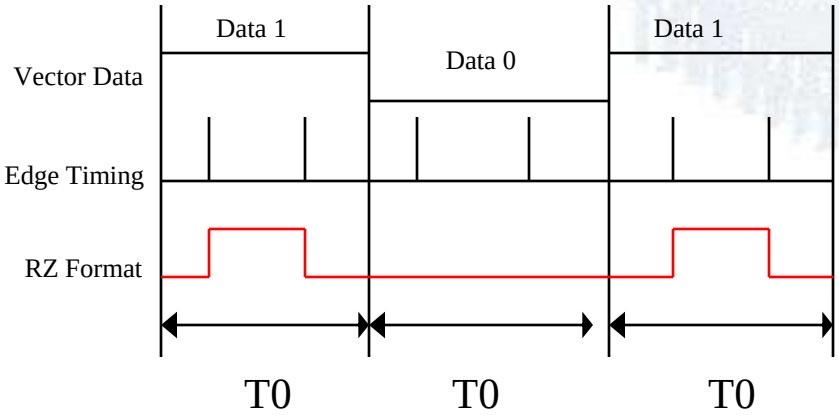
- In the SBC format, data is inverted at the start of the cycle, waits a pre-defined “delay”, presents the actual vector data for the specified pulse width, then inverts the data again for the remainder of the cycle.

How Input Signal is generated ?

- Input data from vector memory is combined with timing, format and voltage level and supplies to DUT via pin electronics.







← Input waveform

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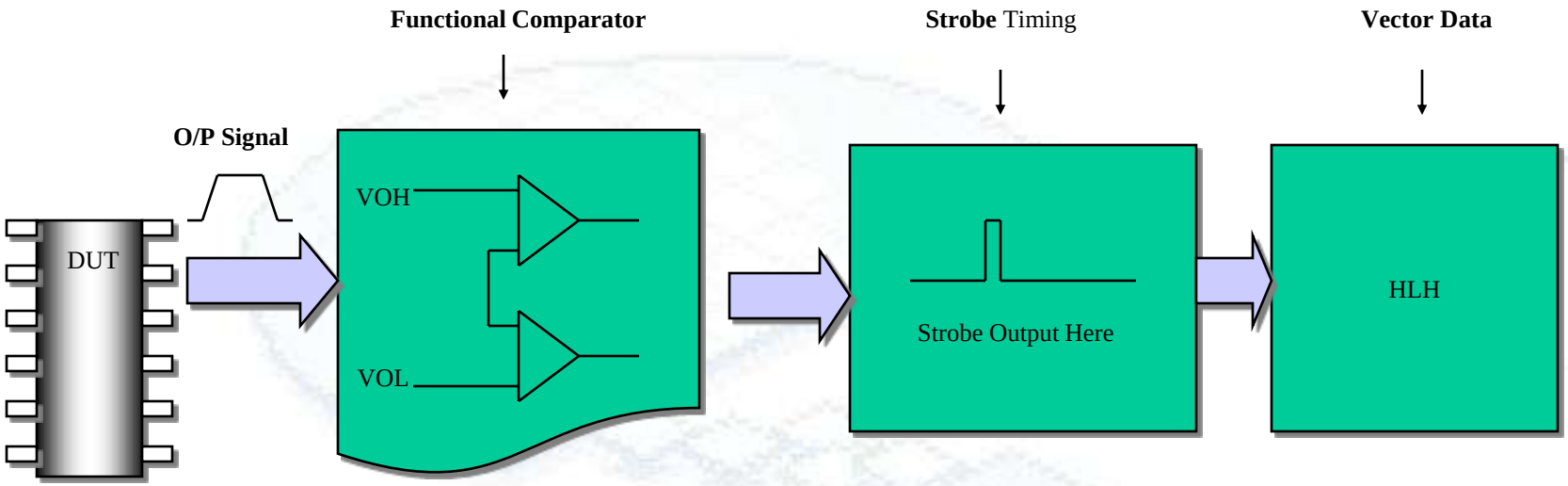
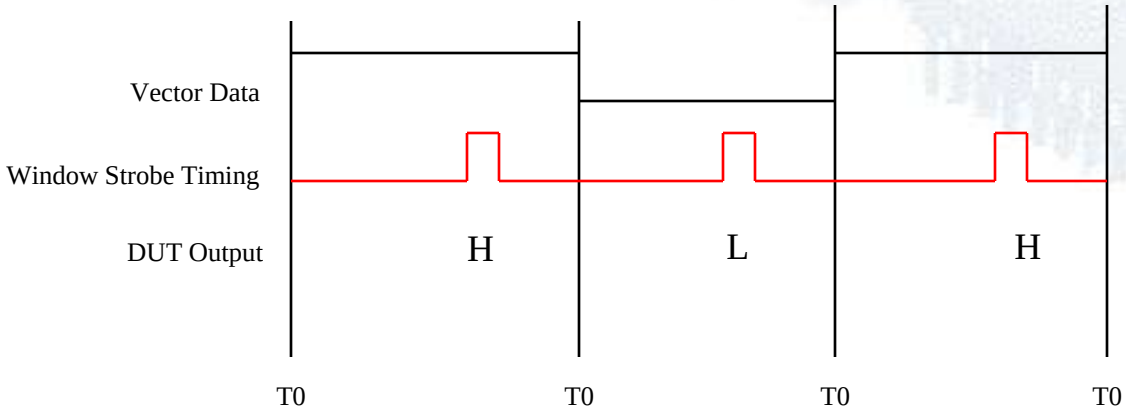
Outputs are Tested By

Output signal waveform comprises of

- Test Vector Data(Expected State)
- Output Strobe Timing (Window strobe, or Edge strobe)
- Output levels - VOL/VOH
- Output currents - IOL/IOH(Output Loading current)

Output Signal Testing





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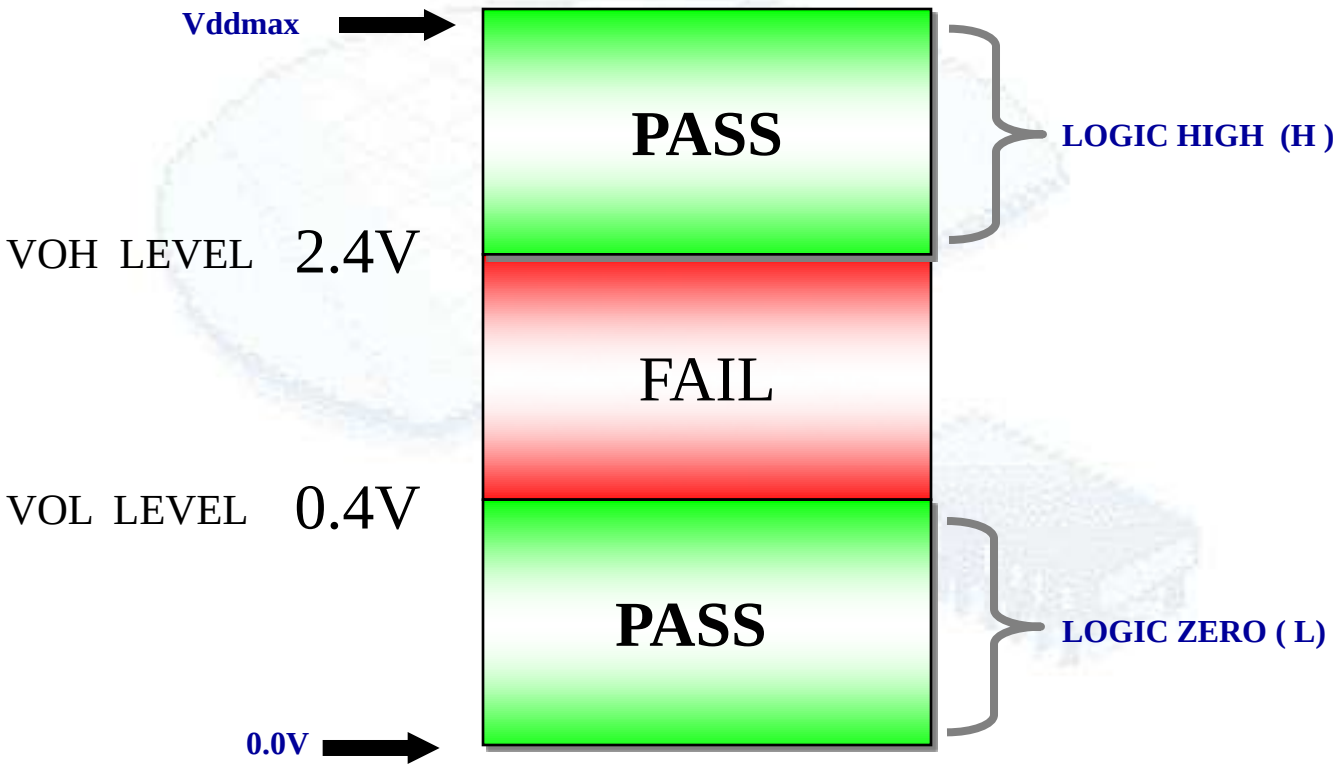
Output Signal Testing

- Output data from DUT monitored via comparator circuit available in pin electronics, and compared with vector memory data at the defined strobe time.

How Outputs Tested ?



Comparator outputs

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Output Test – Strobes

There are two types of strobe markers available for testing the Logic state of the outputs and determine the PASS or FAIL result.

- Edge strobe
- Window strobe

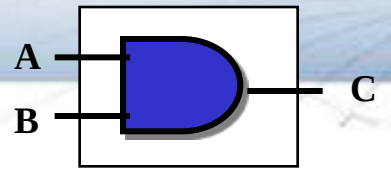
Edge strobe

Edge strobe checks for the output logic state at a single point in time .
Strobe timings are programmed relative to the T0

Window strobe

Window strobe checks for the output logic state during the entire width of the window timing.
Window strobe testing are sensitive for output signals with noise.

Output Test – Edge Strobe



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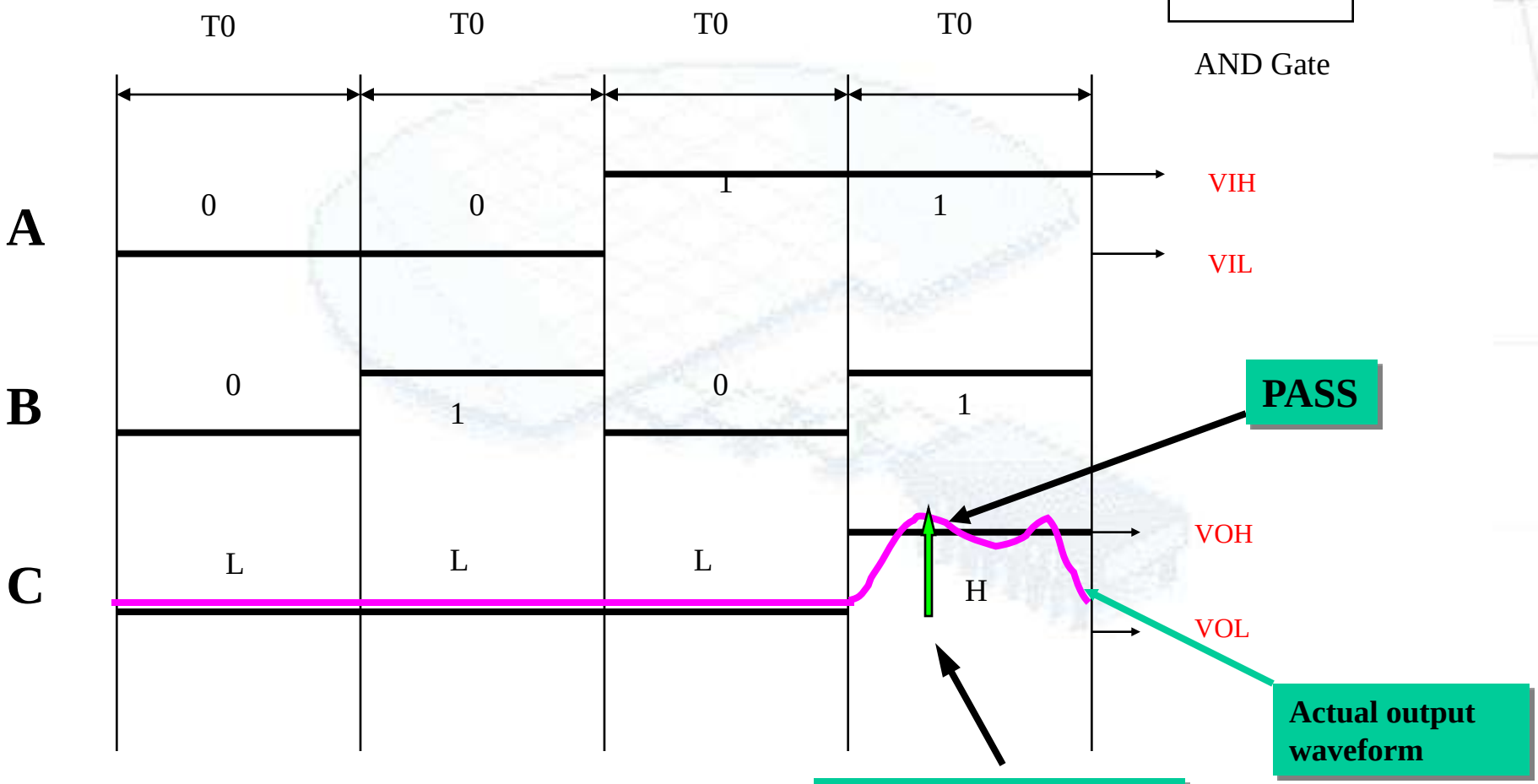

Timing Diagram

Timing Format = NRZ

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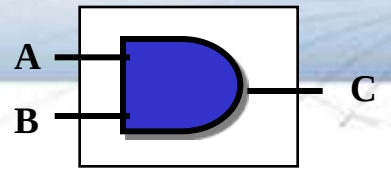
Output Test – Window Strobe



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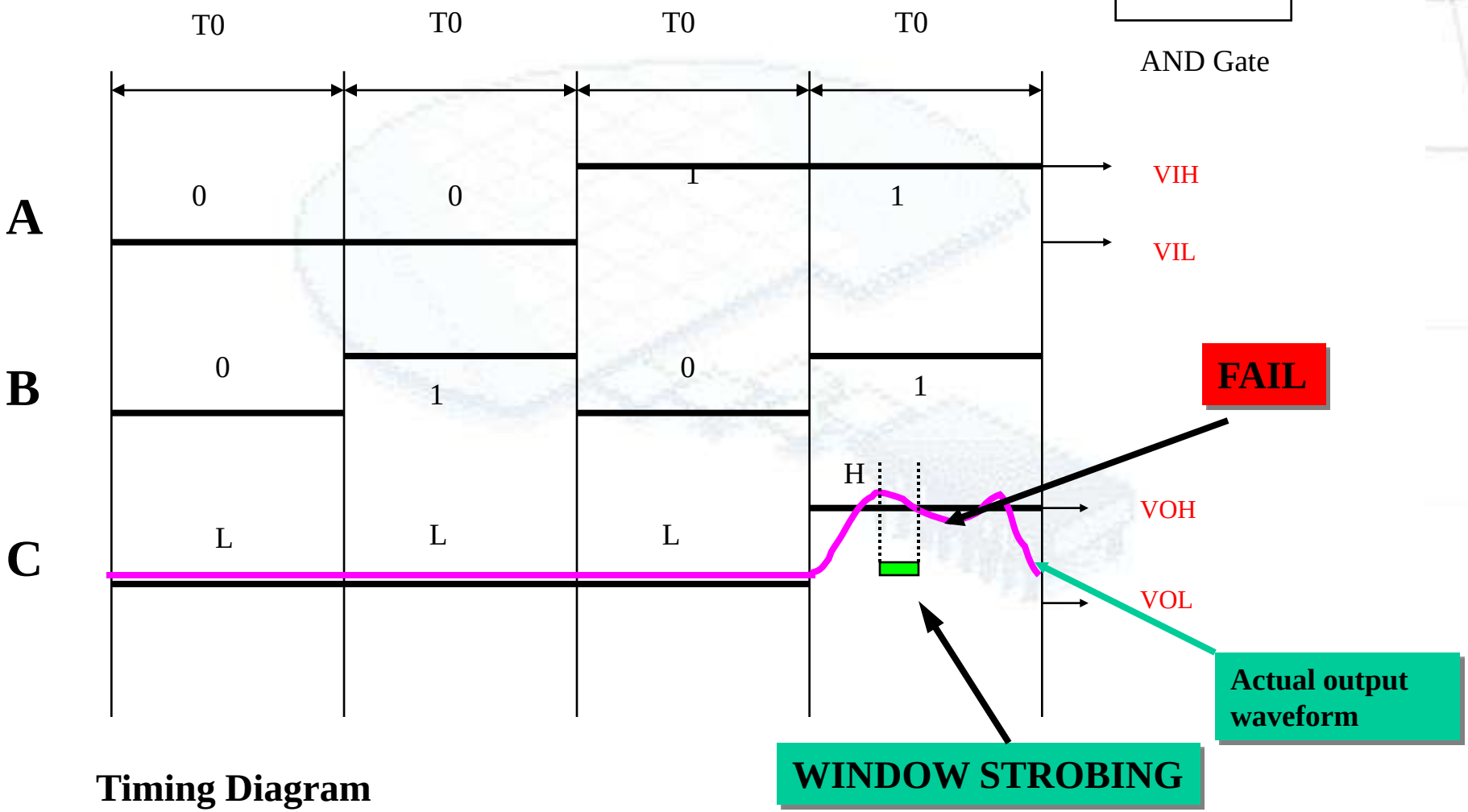

Timing Diagram

Timing Format = NRZ

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Current Loading

- Programmable current loads are used to apply proper IOL/IOH.This helps to measure the DUT's sinking and sourcing capacity.

How Functional Test Works ?

- The Digital subsystem supplies data to the input pins of DUT and monitors its output pins on a cycle by cycle,pin by pin basis.

- If any output pin fails to meet the expected logic state,voltage or timing within the user set tolerance level, the result of the functional test is a failure.

Sequence of Operation

- Define VDD level
- Define input,output levels(VIL/VIH/VOL/VOH)
- Define output Current Loading(IOL/IOH)
- Define Test Cycle Time (Frequency)
- Define timings and formats for all input pins
- Define output strobe timing for all output pins
- Define start and stop locations for memory
- Execute the test

Test Concepts

- There are two methods used to functionally verify device specifications:
  1. Gross functional test
  2. Standard functional test

Gross Functional Test

- Gross functional test or wiggle test performs a functional test with relaxed conditions.
- Frequency, timings, voltages and current loading are generally relaxed.
- This test indicates whether or not the DUT is functionally ‘alive’.
- It is often executed early in the test program flow and is used to verify correct functionality of all test vectors which will be throughout the entire test program.

Standard Functional Test

- Standard functional test is used to functionally verify a given parameter.
- Each unique circuit design requires an unique set of functional test conditions.
- These tests may be executed at different VDD levels, VDDmin, VDDmax, VDDnom levels specified in the data sheet
- Most of the tests are done at the maximum operating frequency of the device .

Test Concepts

Input Stimulus:-

- Pattern data per DUT input requirements

Expected Response:-

- Pattern data per DUT output requirements

Test Condition(s):-

- Required power supply voltage setting as defined in datasheets

VIL/VIH Functional Test

- VIL is the max-voltage applied to an input to represent logic 0, while VIH is the min-voltage to represent logic 1
- VIL/VIH test guarantees that the input pins can correctly sense/differentiate the proper logic levels
- This test is performed by applying the specification-defined input levels, and then executing a functional pattern.

Parameter	Description	Test conditions	Min	Max	Units
VIH	I/P High voltage		2.2		V
VIL	I/P Low voltage			0.8	V

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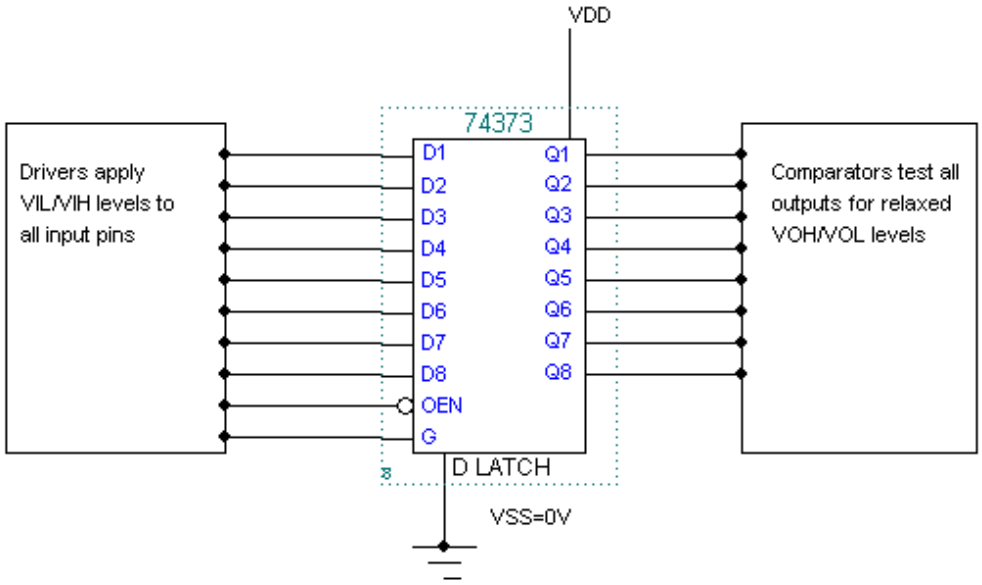
VIL/VIH Level Test



Set the input levels as per the spec
Execute the functional test relaxing all the other parameters and frequency.
Output levels also need to be relaxed
Functional pattern outputs will fail if the input level does meet the specification
Test can be executed at VDDmax and VDDmin

VIL/VIH Troubleshooting

- Relax VIL values towards 0 and VIH values towards VDD and try different permutation combinations
- It may be necessary to eliminate all output loading and to reduce the test frequency and test it in a noise free environment.

VIL/VIH Key points…

- Purpose:To verify that the input buffers will properly detect VIL,VIH voltage levels
- VIL,VIH can only be verified by executing a dynamic functional test
- Test limits are defined in device specification (often as DC spec)
- Output pins fails as a result of improper operation of input circuitry

VOL/IOL, VOH/IOH Testing

- VOL/IOL ,VOH/IOH test guarantees that the output pins can correctly maintain their Output logic level at the specified sink/source current.

- During functional test execution, output pins are loaded (apply IOL/IOH) to check their sink/source capacity. The resultant voltage is compared to the set VOL/VOH

Parameter	Description	Test conditions	Min	Max	Units
VOH	O/P High voltage		2.4		V
VOL	O/P Low voltage			0.4	V

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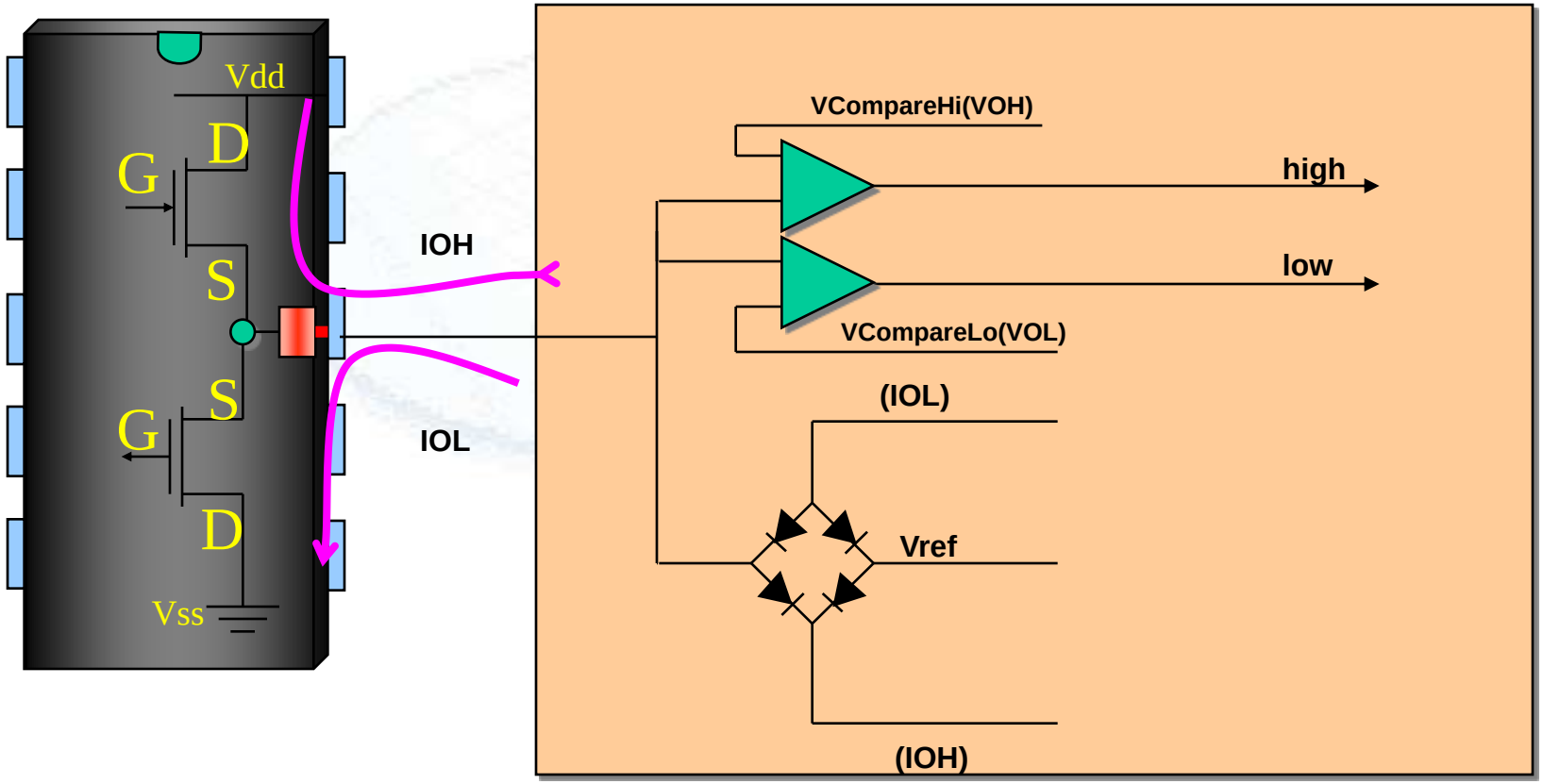
Functional VOL/VOH Test



Set the VOL/VOH, IOL/IOH to the specification's values
Execute the functional pattern, and check the outputs

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VOL/IOL, VOH/IOH Troubleshooting

- With the help of datalog identify the device pin tat failed and the failing state. Relax the VOL/VOH levels. IOL/IOH levels can also be relaxed to make the device pass

VOL/VOH Key Points…

- Purpose is to verify that the output buffers will properly supply the correct amount of output current and voltages
- Dynamic functional test is executed
- Test limits are defined as in device specification
- Test requires current load on output pins
- It may not be possible to test all output pins simultaneously when fully loaded, due to noise produced by high currents

Test Vectors

- Test vectors represents the input and output states which represents the logical functions that the DUT has to perform.
- Input data are represented by character 0 / 1.
- Test vectors are called as test patterns or truth tables.
- Output data are represented by L / H / Z and X.
- Test vectors are stored in Vector memory

Test Vectors

- Input data from vector memory is combined with timing, format and voltage level and supplies to DUT via pin electronics.
- Output data from DUT monitored via comparator circuit available in pin electronics, and compared with vector memory data at the defined strobe time. This type of testing is called stored response
- In addition to DUT data, instructions to the test systems are also available in test vector sequence.
- Timing settings and signal formats may change on a vector by vector basis.
- Most ATE systems support microcode instructions to perform looping, jumping and subroutines etc.

Sample Vector File

```
// Functional Patterns
import tset time_ANDPattern;
vector ($tset, A,B,C)
{
global func_start_ANDPattern:

            >time_pattern   0 0 L   ;
            >       -           0 1 L  ;
            >       -           1 0 L  ;
            >       -           1 1 H  ;

Func_stop_ANDPattern: halt

}
```

Roles in Creating Vectors

- Design engineer will be most familiar with functions of device and mostly responsible for vector generation also.
- Test engineer has to discuss with designer about the detail of testing, review of timing and voltage requirements and discuss about the length/depth of test vector.

Roles in Creating Vectors

- Test vectors for complex devices are typically extracted from simulation data created during the design process.
- These are typically created by design/test/simulation engineer with the help of simulation tools
- Simulation data may need to be reformatted for use on test system.
- Using macros, engineer should try to automate the test vector generation rather than manual.

Tester Memory

- Test Vectors are stored in Vector/Pattern Memory.
- The size of the test vector memory determines the number of vectors that can be executed at any one time.
- If the memory is small, Test Vectors need to be reloaded many times - increase the overall test time.

Self-Assess Questions

1. Name at least 3 Digital Input Signal Format

2. How many timing edges do you need if you want to do a window strobe?

3. Which of the below refer to inputs on your test vectors?
   1, 0, H, L, Z

4. When an engineer says the vector frequency is 30MHz. You would expect this value defined in Timeset or Edgeset? What is the period then?

5. In Digital Functional Testing, input stimulus, and output compare is performed by the Digital Subsystem. These will in turn control the levels and timing affecting the test. What is another aspect that will affect the Functional Testing other than Levels and Timings?

AC PARAMETERS TEST

Purpose / Why

The purpose of the AC Parameters test is to guarantee that the device meets all its timing specification specified in the device datasheet.

The AC Timing Test verifies the following timing parameters:

1. Period, Frequency, Rise Time, Fall Time, Setup time, Hold time, Pulse Width, Propagation Delay, etc

2. These parameters are tested under recommended conditions listed by the Datasheet and compared against the Datasheet values.

Test Method

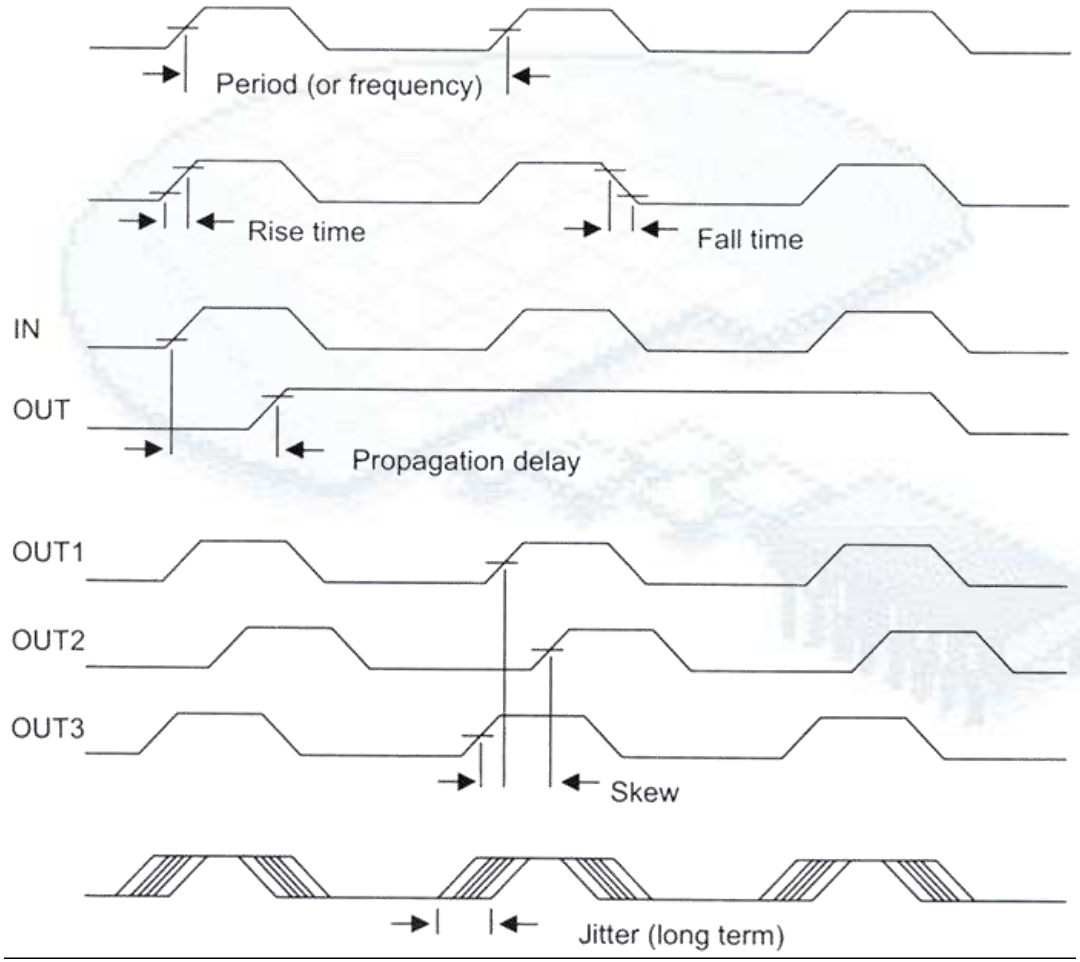
AC Parameters can be verified functionally.

For high speed devices, AC timing parameters can be set to their worst case conditions and a functional test executed .

This Go/No-Go test, is a faster, and usually used in production testing, to check that the device meets the design specification.

To measure the operating limits of the AC parameters, Characterization methods can be used

AC Timing Parameters

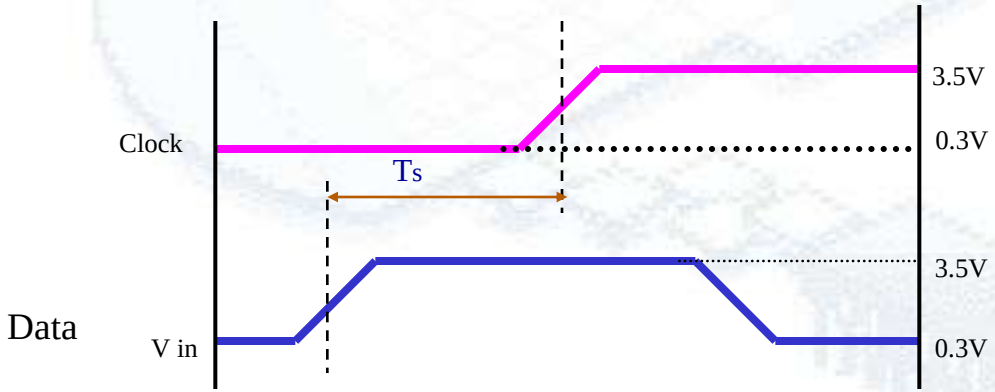


Revised 8/8/2007

Setup Time

Setup Time

The time needed by the signal/data to remain stable before the clock is triggered in order to guarantee proper output data

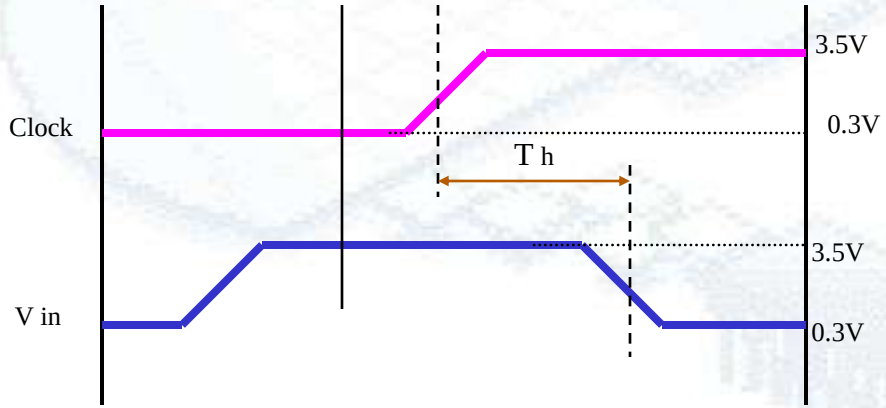


- Performed only on input pins

Hold Time

Hold Time

The time needed by the signal/data to remain stable after the clock is triggered in order to guarantee proper output data

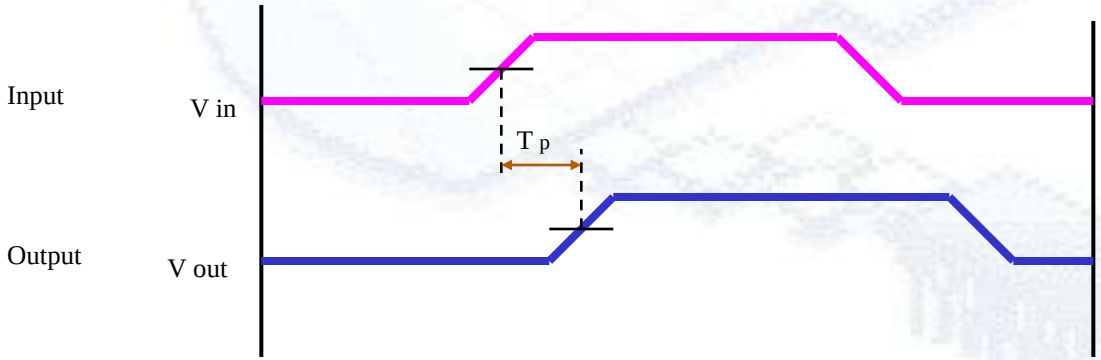


- Performed only on input pins

Propagation Delay

Propagation Delay

Propagation delay time is the amount of time that it takes for a change in an input signal to produce a change in the output signal measured at a specific voltage level.



- Propagation delay measurements are made from an input pin to an output pin.

Transition Time

The time that the output logic take to change from one state to another is called *transition time*.

Transition time has two components…

- Rise time (tr)
- Fall time (tf)

The rise and fall times of CMOS outputs depend on the resistance of the “on” transistor and the load capacitance.

The load capacitance comes from…

- Input capacitance of load device
- Wire connecting the output to its inputs
- Board capacitance.

Transition Time

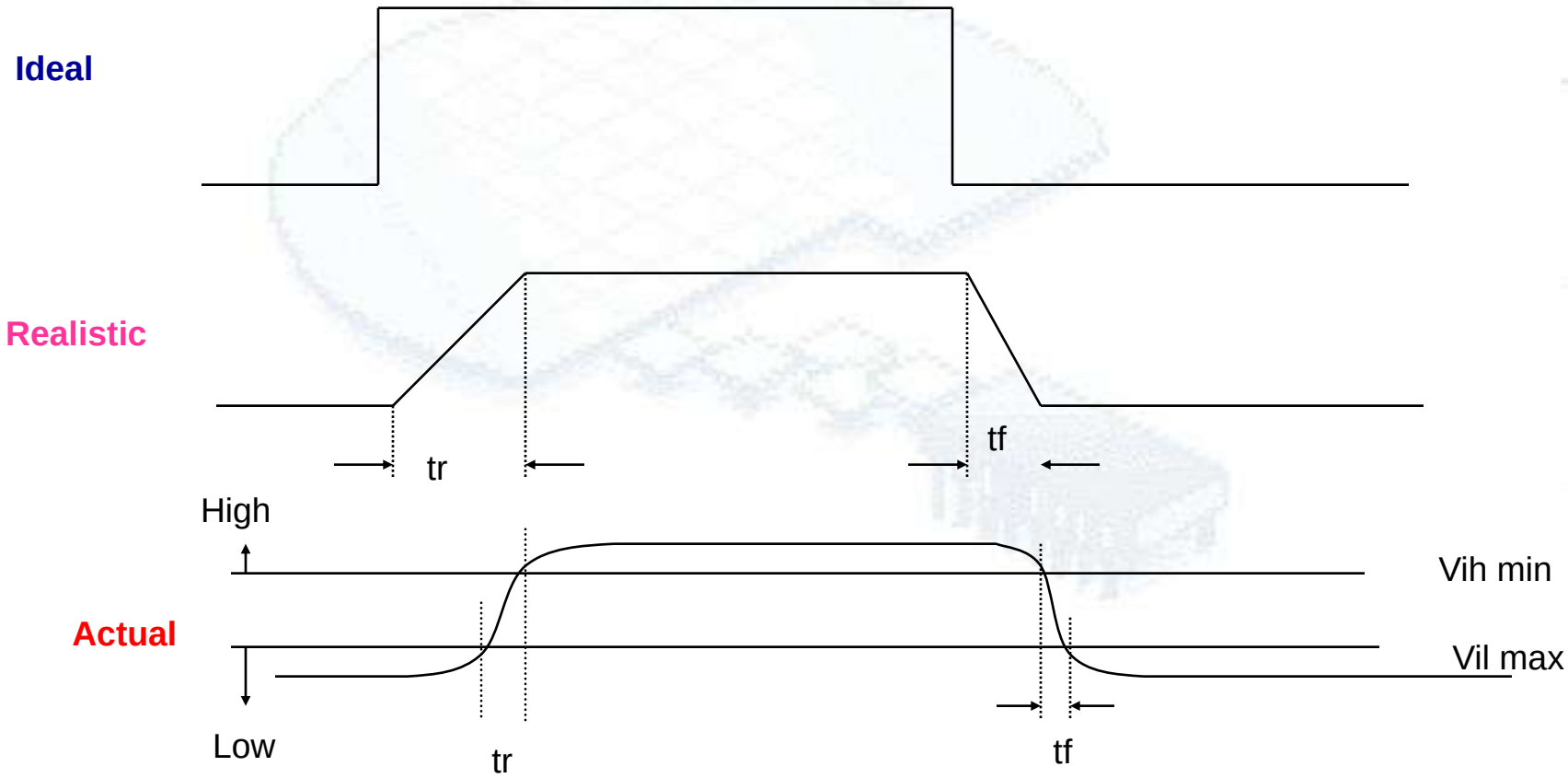
Rise Time

The time required for an edge to go from (typically) 10% to 90% of its high limit voltage value

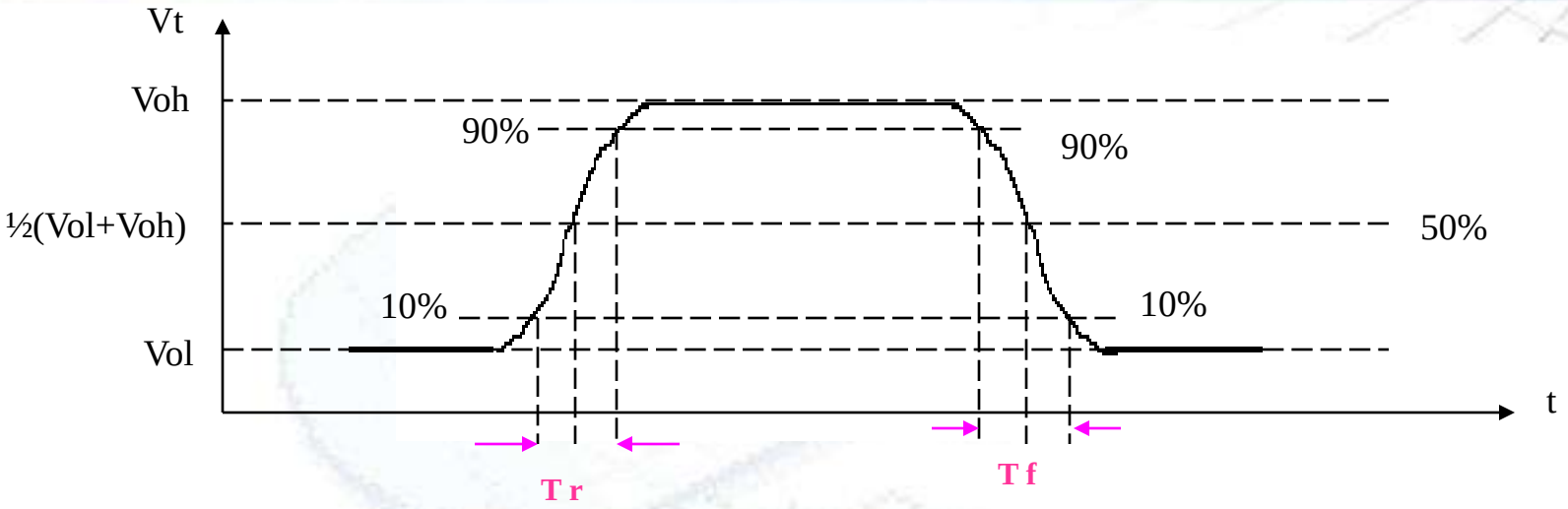
Fall Time

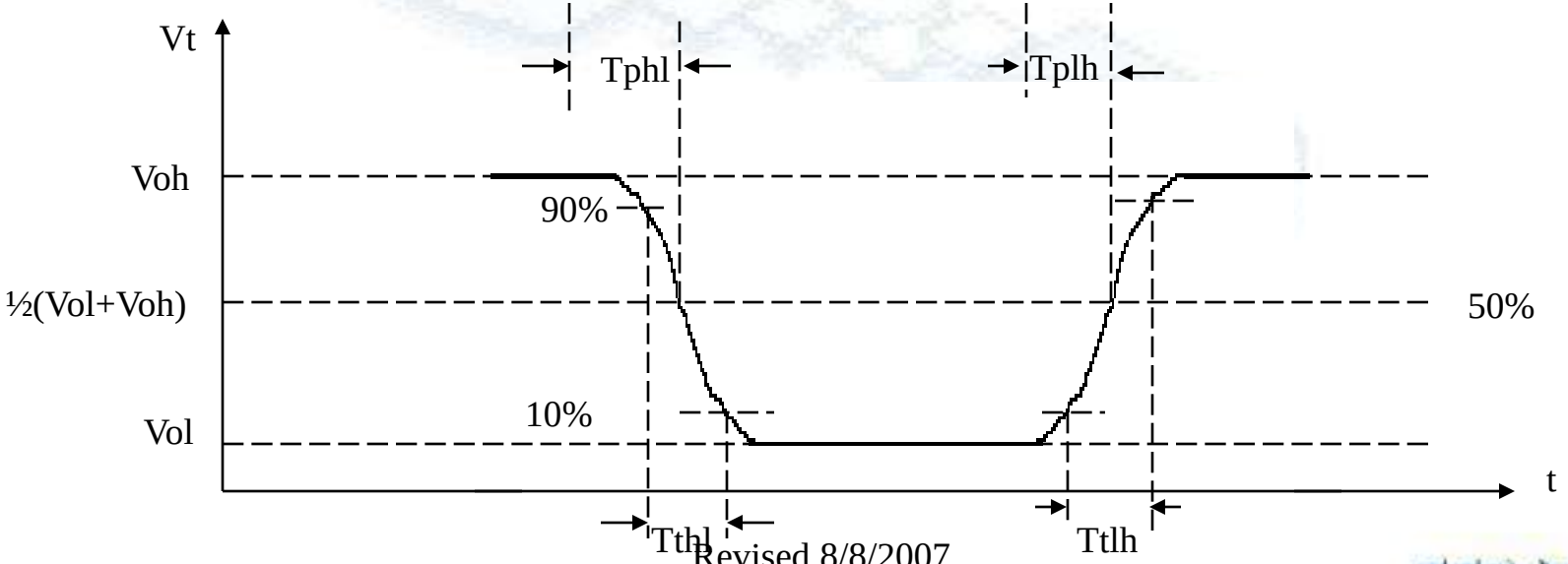
The time required for an edge to go from (typically) 90% to 10% of its low limit voltage value

Transition Time
Rise Time / Fall Time



Rise Time / Fall Time

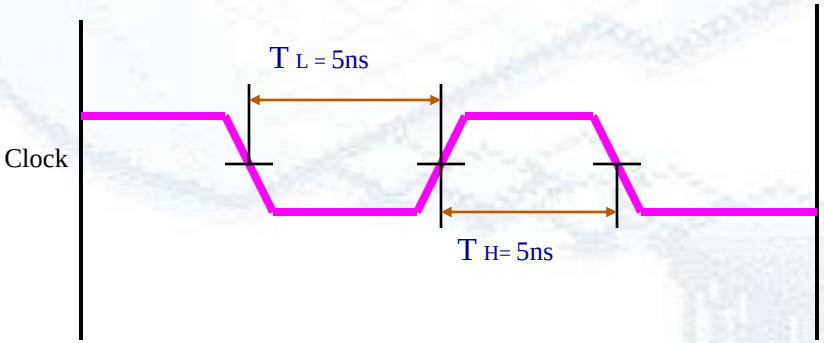




Maximum Frequency

Max Frequency

The maximum operating frequency is usually the inverse of the sum of the minimum clock low and clock high times



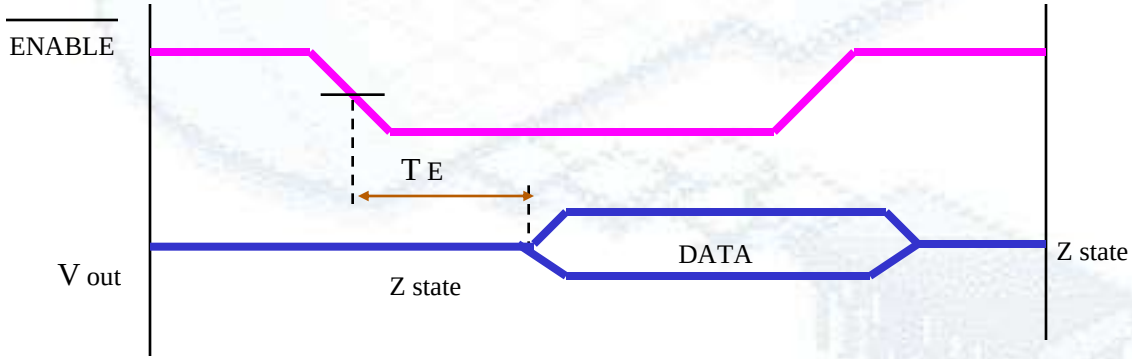
Freq = 100 MHz

- It guarantee the maximum device operating frequency.

Output Enable Time

Output Enable time

Output enable time is the time it takes an output to switch from high impedance state to driving valid logic levels.

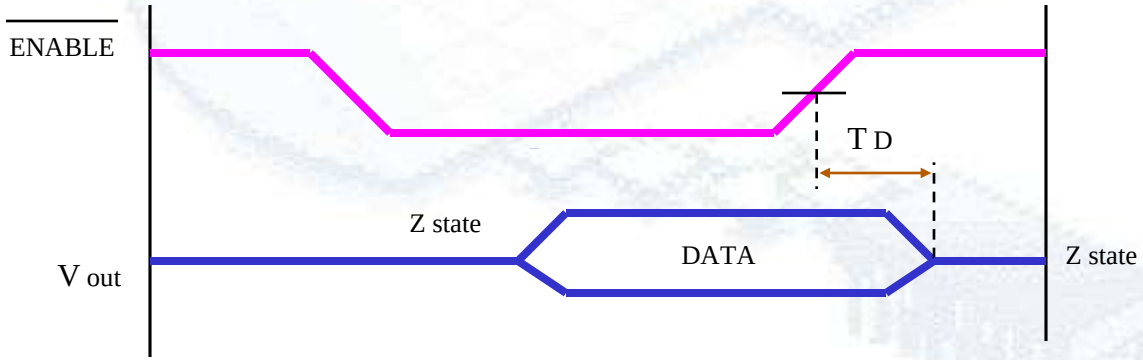


- This test is done on high impedance outputs and bi-directional device pins.

Output Disable Time

Output Disable time

Output disable time is the time it takes an output to switch from driving valid logic level to a high impedance state.



- This test is done on high impedance outputs and bi-directional device pins.

AC Specification – Data sheet

74ABT373

AC Electrical Characteristics

(SOIC and SSOP Packages)

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	1.9	2.7	4.5	1.0	6.8	1.9	4.5	ns
t_{PHL}	D_n to O_n	1.9	2.8	4.5	1.0	7.0	1.9	4.5	
t_{PLH}	Propagation Delay	2.0	3.1	5.0	1.0	7.7	2.0	5.0	ns
t_{PHL}	LE to O_n	2.0	3.0	5.0	1.5	7.7	2.0	5.0	
t_{PZH}	Output Enable Time	1.5	3.1	5.3	1.0	6.7	1.5	5.3	ns
t_{PZL}		1.5	3.1	5.3	1.5	7.2	1.5	5.3	
t_{PHZ}	Output Disable Time	2.0	3.6	5.4	1.7	8.0	2.0	5.4	ns
t_{PLZ}		2.0	3.4	5.4	1.0	7.0	2.0	5.4	

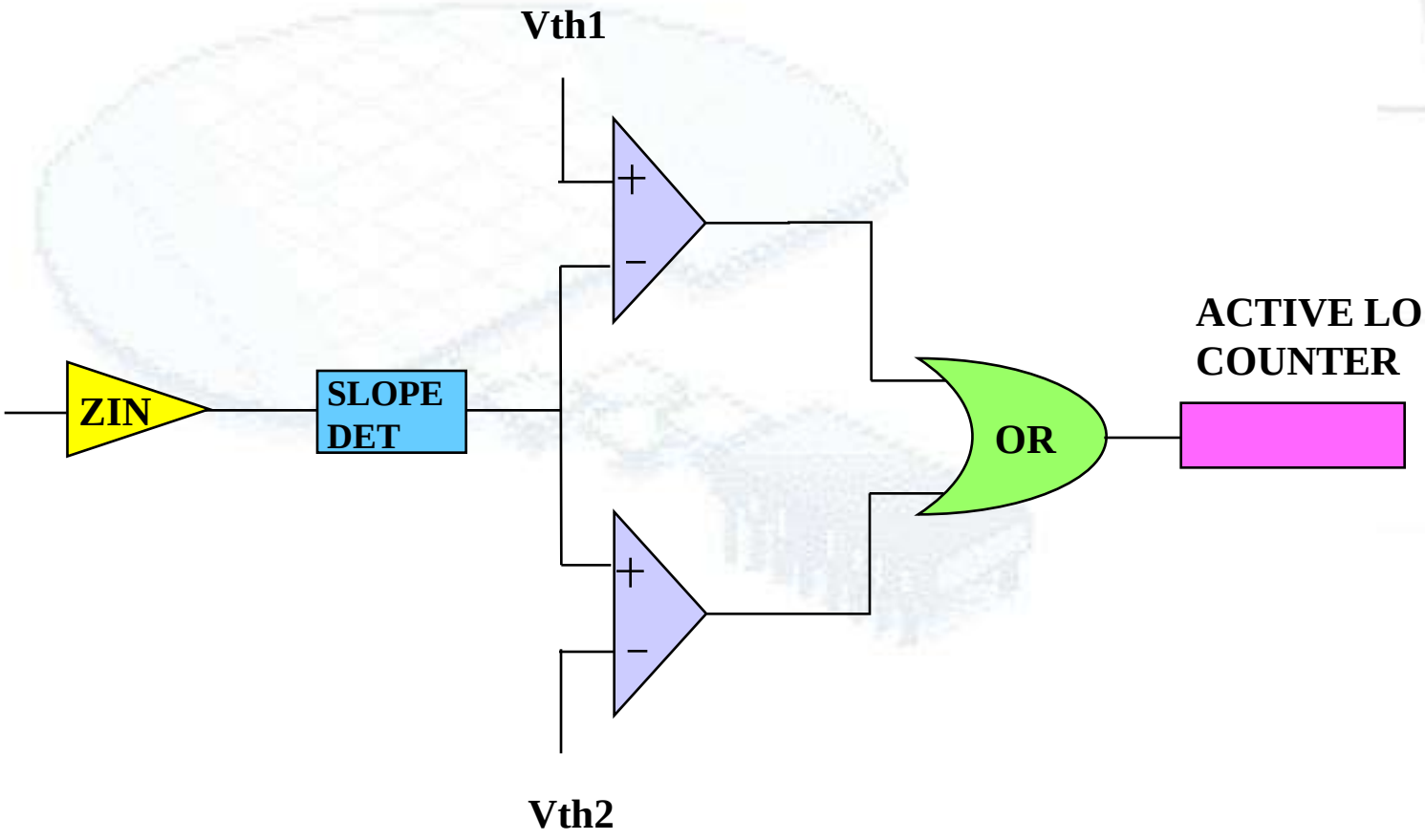
AC Operating Requirements

(SOIC and SSOP Packages)

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{TOGGLE}	Max Toggle Frequency		100		100				MHz
$t_S(H)$	Setup Time, HIGH	1.5			2.5		1.5		ns
$t_S(L)$	or LOW D_n to LE	1.5			2.5		1.5		
$t_H(H)$	Hold Time, HIGH	1.0			2.5		1.0		ns
$t_H(L)$	or LOW D_n to LE	1.0			2.5		1.0		
$t_W(H)$	Pulse Width, LE HIGH	3.0			3.3		3.0		ns

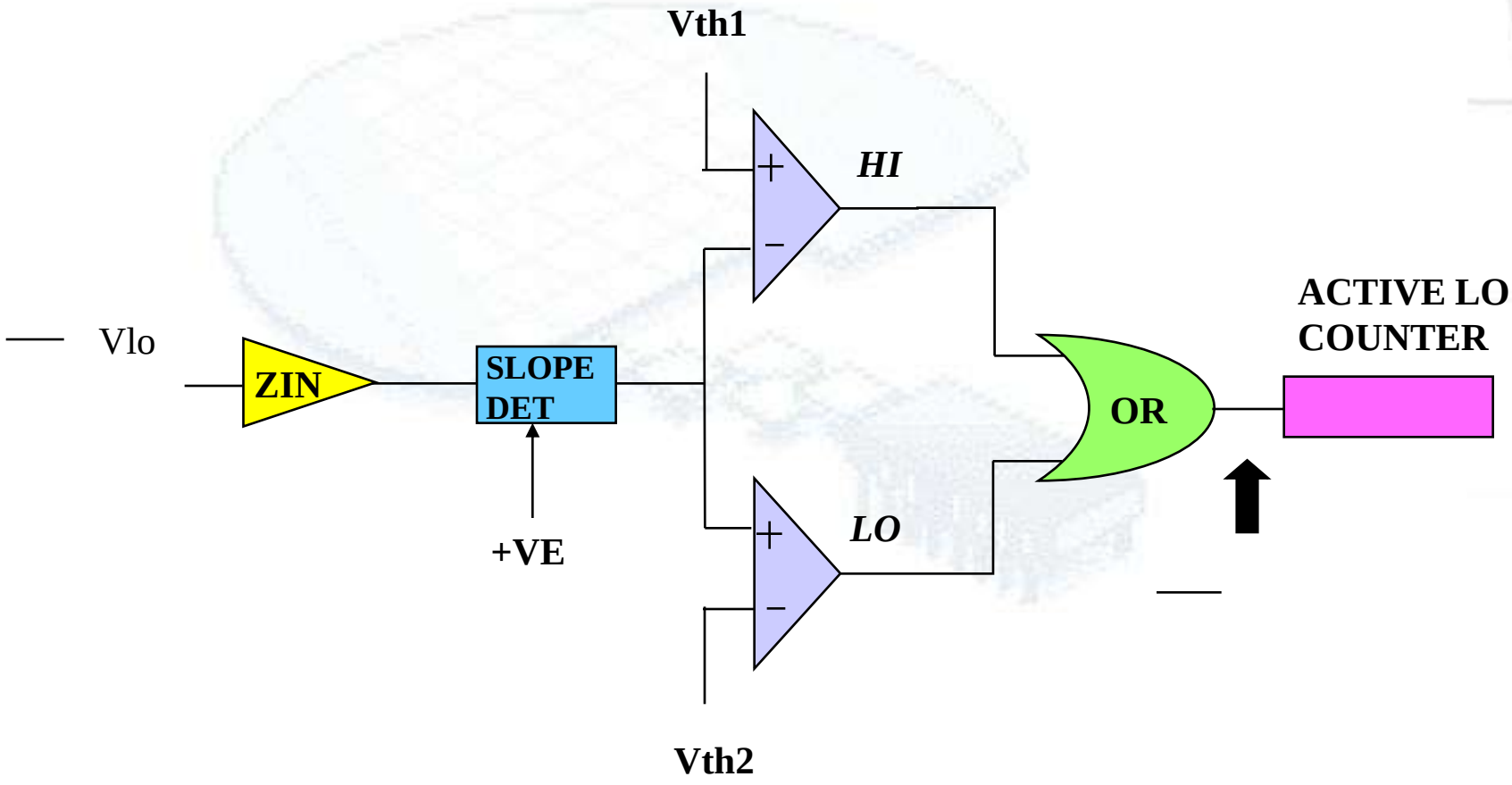
Revised 8/8/2007

TIME MEASUREMENT SUBSYSTEM (TMS)



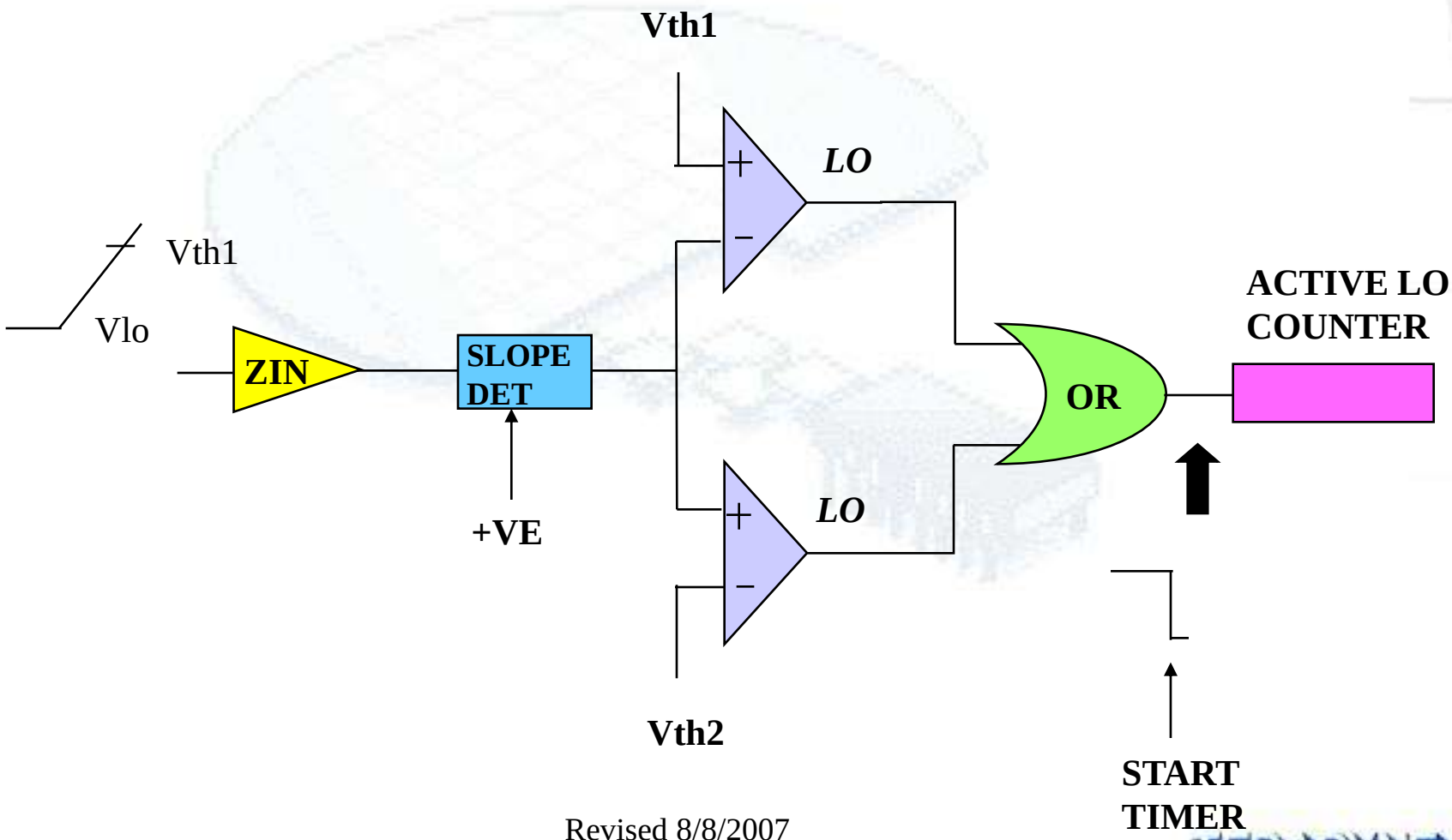
Revised 8/8/2007

TMS OPERATION
(RiseTime/SlewRate)

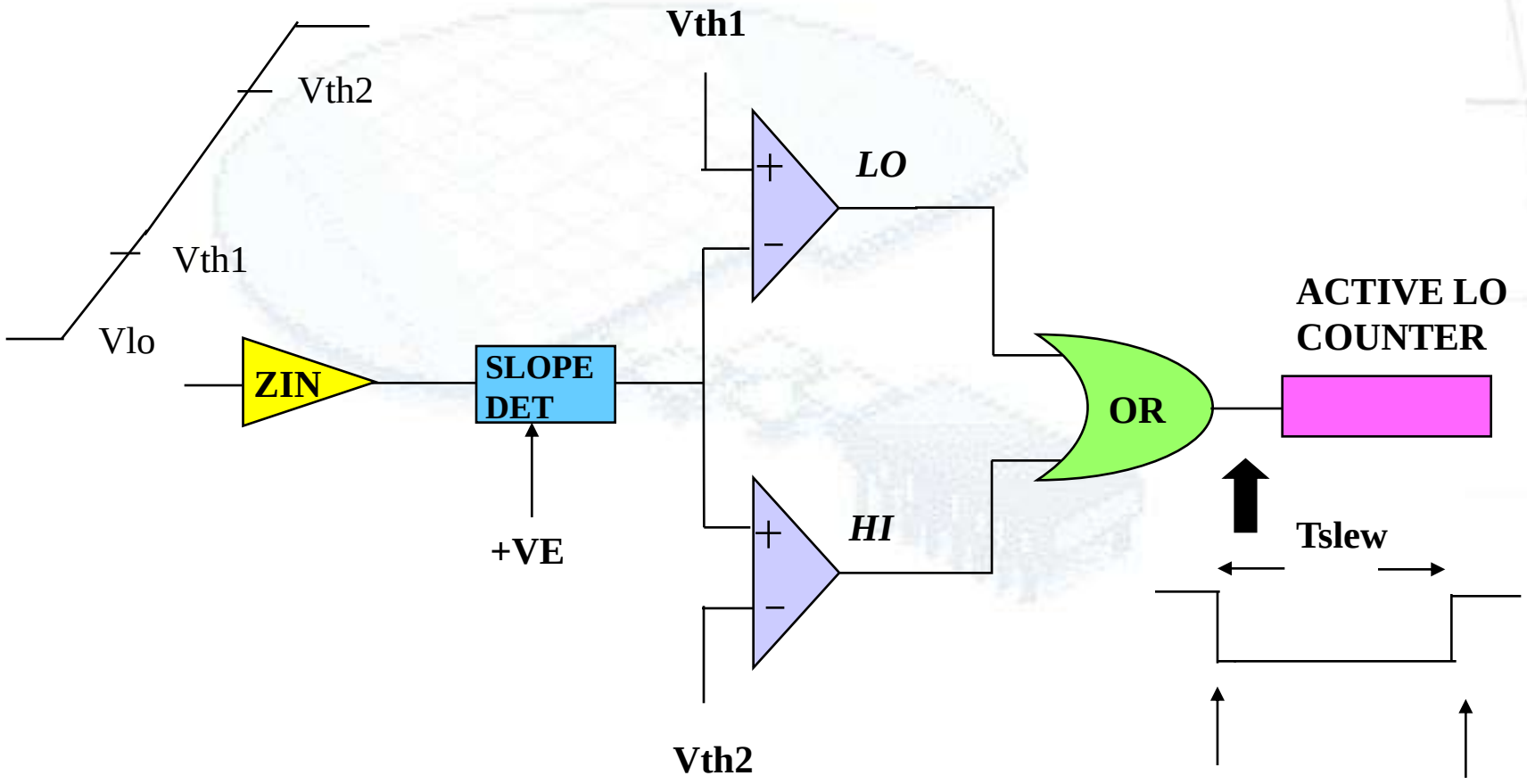


Revised 8/8/2007

TMS OPERATION
(RiseTime/SlewRate)

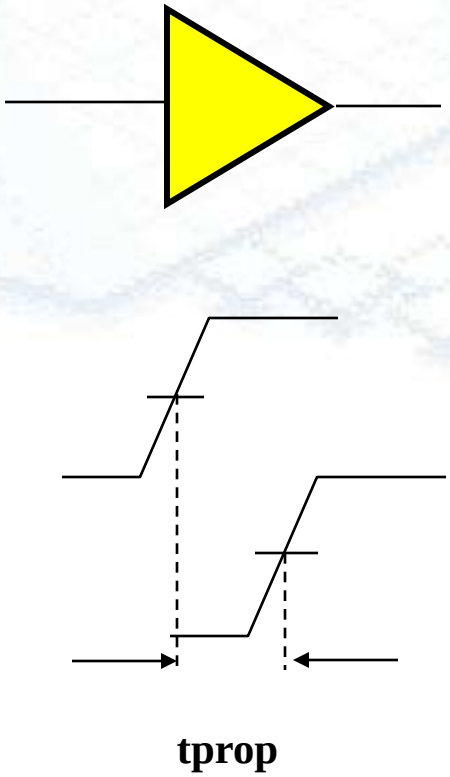


TMS OPERATION
(RiseTime/SlewRate)

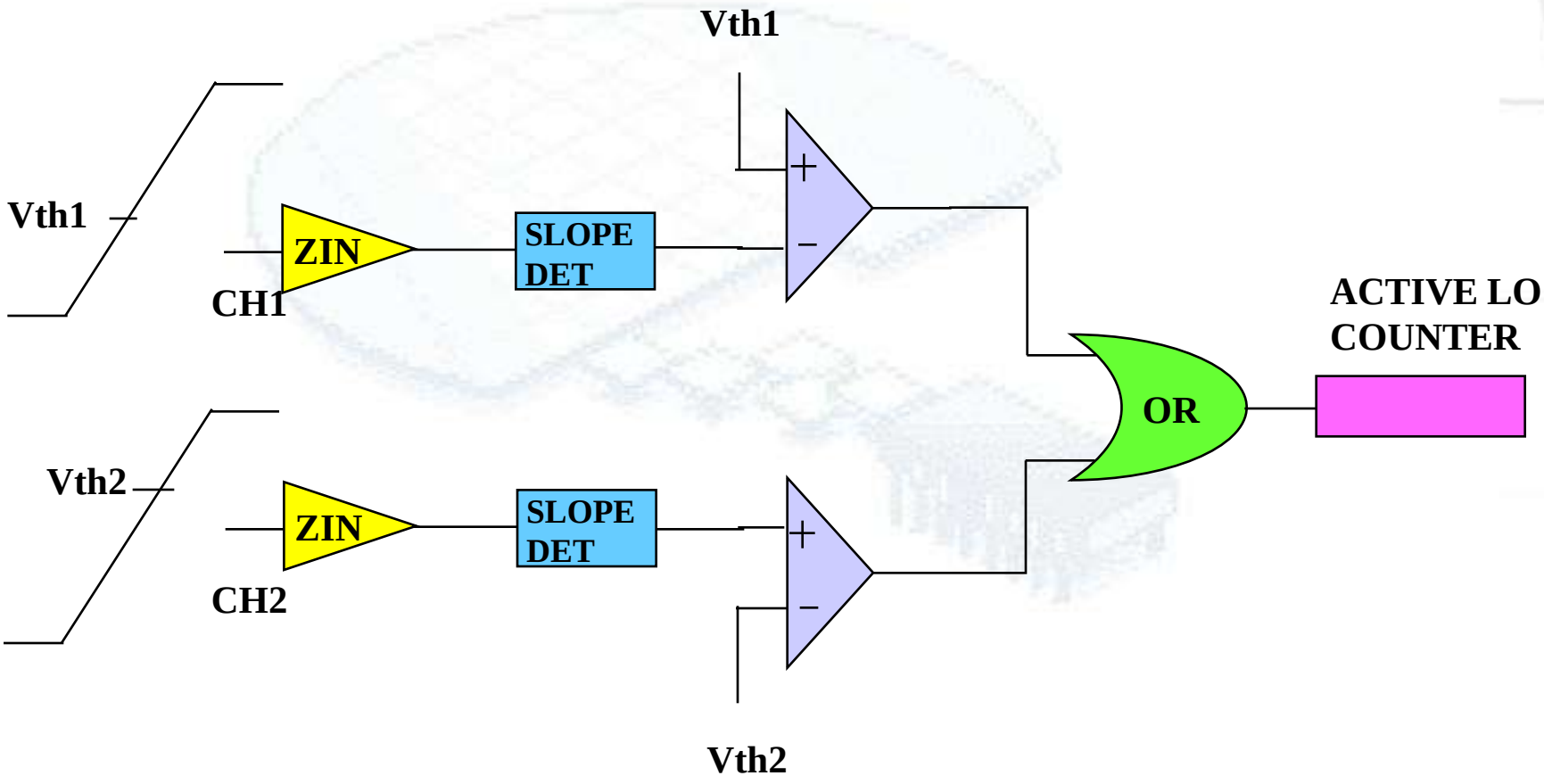


TMS OPERATION
(Propagation Delay)

High amplitude fast edge at input of OpAmp drives the OpAmp to slew limiting. In this condition, the response is a linear rise in voltage.

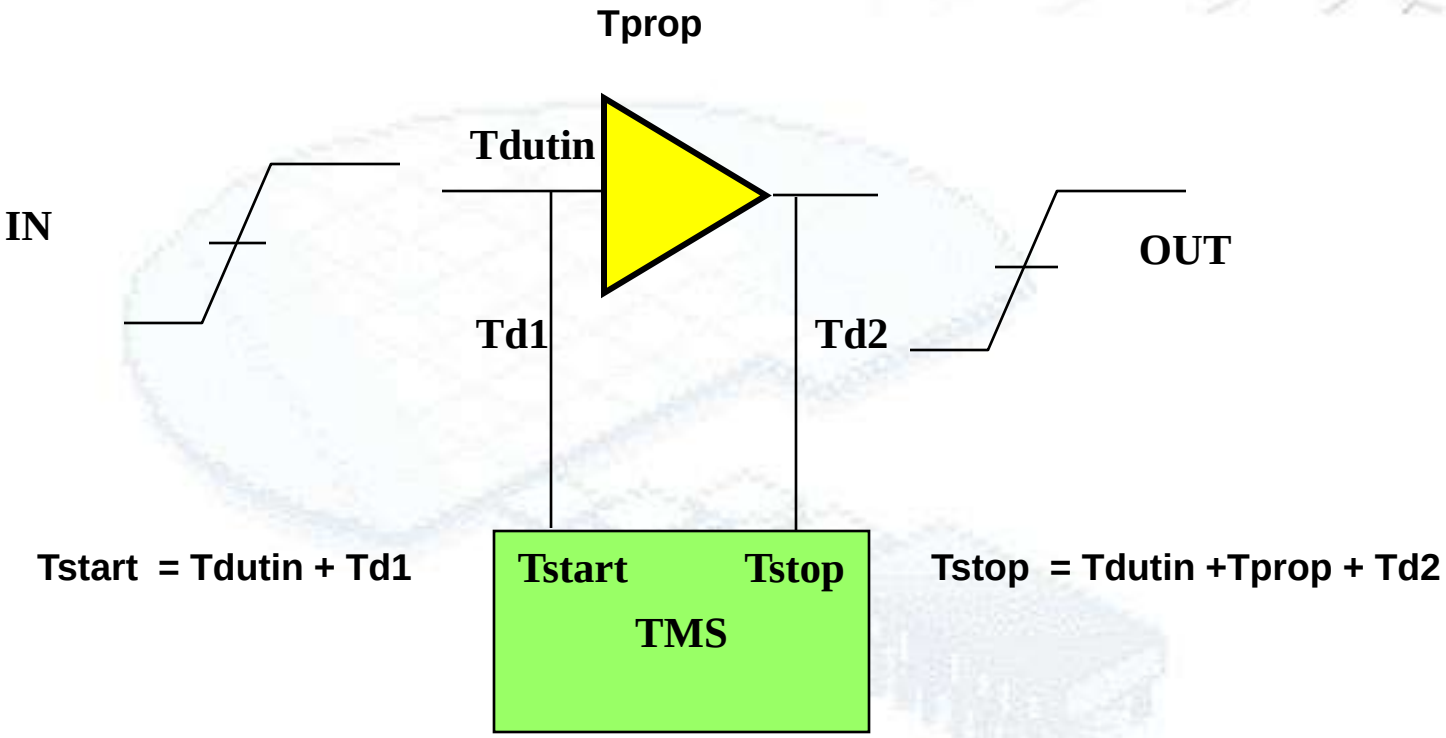


TMS OPERATION (2-channel TMS)
(Propagation Delay)



Revised 8/8/2007

TIMING CALIBRATION
PATH SKEW / DE-SKEW

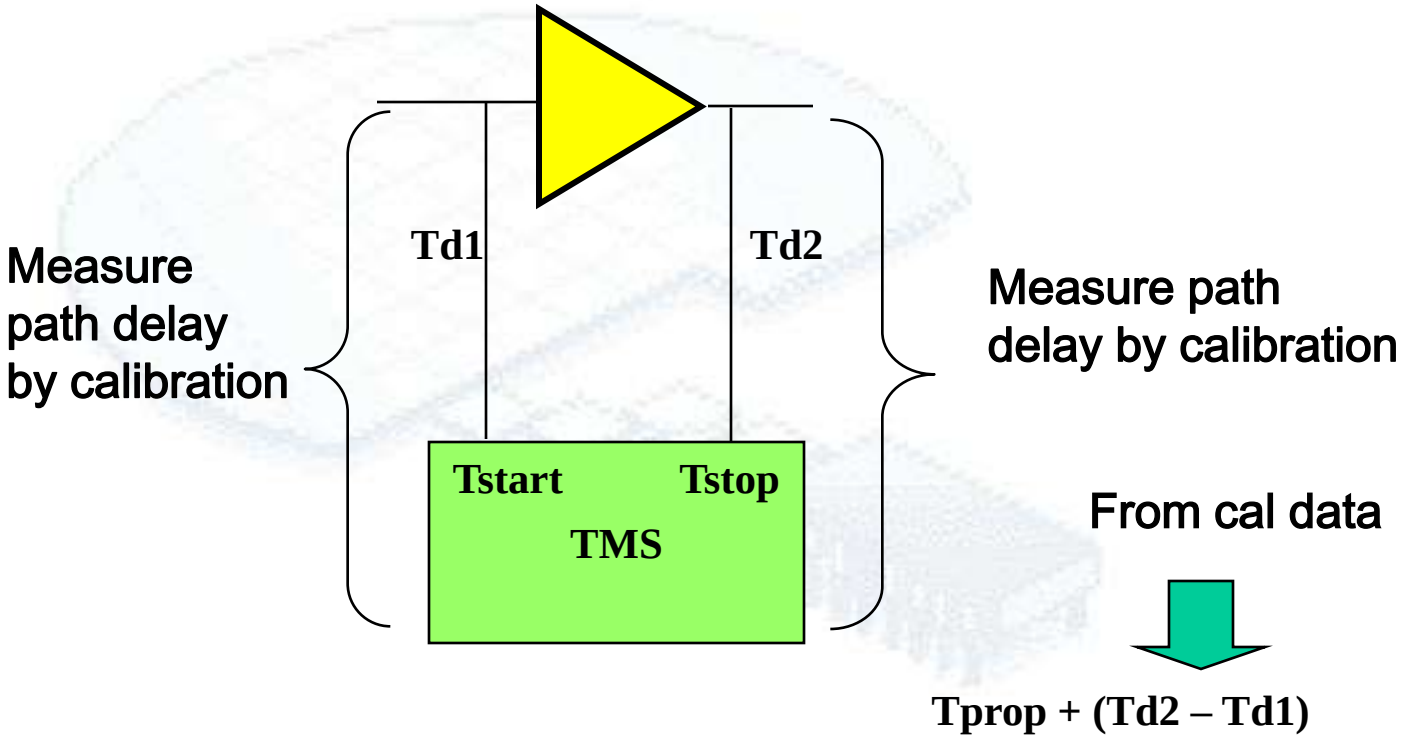


Time interval = Tstop – Tstart
= (Tdutin + Tprop +Td2) – (Tdutin + Td1)
= Tprop + (Td2 – Td1)

Skew = Td2 – Td1

Revised 8/8/2007

PATH SKEW / DE-SKEW



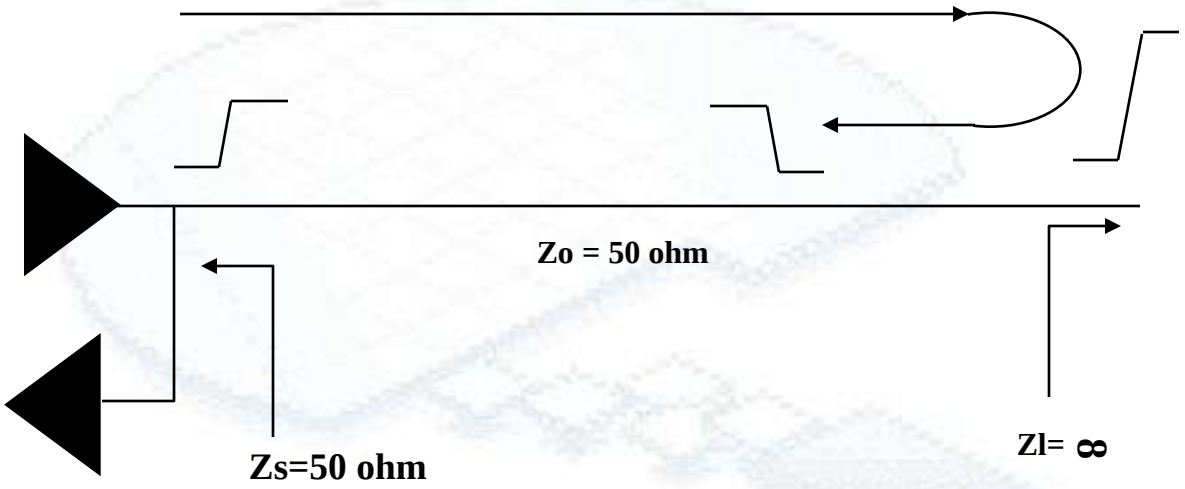
Path de-skew is done by measuring Td1 and Td2 or Td2-Td1 via tester calibration if the paths are tester internal paths. If the paths are user designed paths (DIB traces), then either a TDR (if these are HSD paths) is done to get Td1 and Td2, or the traces are designed to match in exact dimensions, so as to make Td1=Td2.

PATH DELAY (TDR calibration)

There is a finite time between an edge occuring at the driver in the channel card, and at the DUT. It takes Tpd time for the edge above to reach the DUT. When assigning edge values to the tester, we need to compensate for this Tpd.

The path delay are made up of the channel coax cables, the tester to DIB contact, the DIB trace to DUT socket. It is important that this path have a characteristic impedance of 50 ohm to prevent reflections along the path.

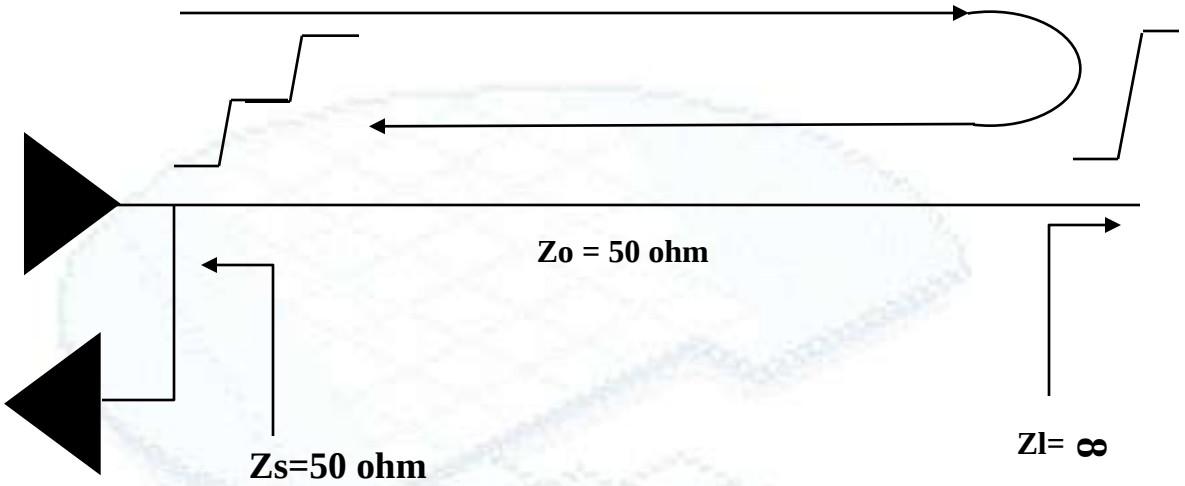
PATH DELAY (TDR calibration)



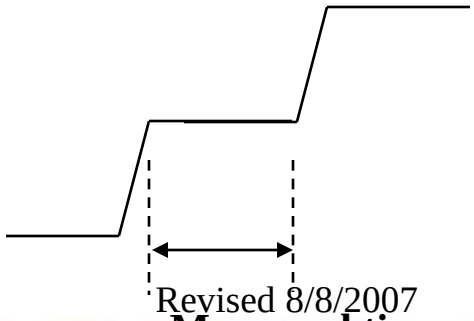
The typical technique used by most ATEs to measure out the path delay is called Time Domain Reflectometry or TDR. Here, the DUT is not part of the setup, so the line is open circuit at the end. This causes the edge sent by the driver to get reflected back at 0 phase shift.

Vref/Vinc = (Zl – Zo) / (Zl + Zo).For Zl= ∞ , Vref = Vinc.

PATH DELAY (TDR calibration)



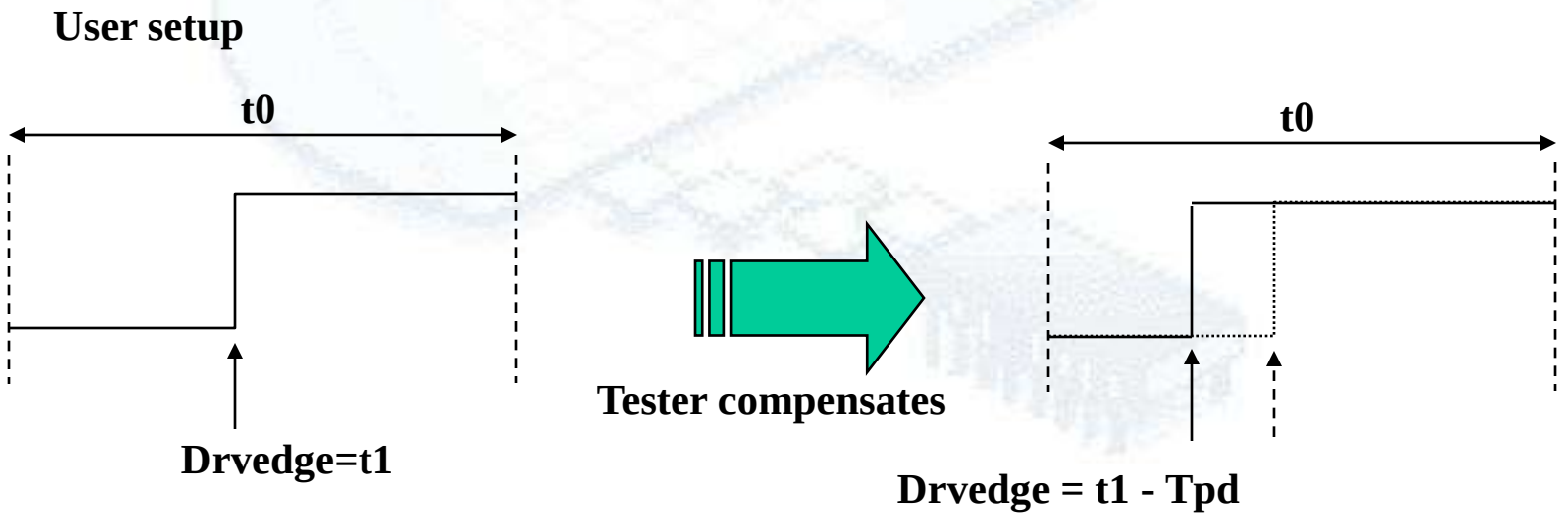
The total path of the signal from source to open end and back to the source is called the round-trip delay.The reflected edge superimposes with the voltage at the source at time = 2xTpd:



Measured time= 2xTpd

PATH DELAY (TDR calibration)

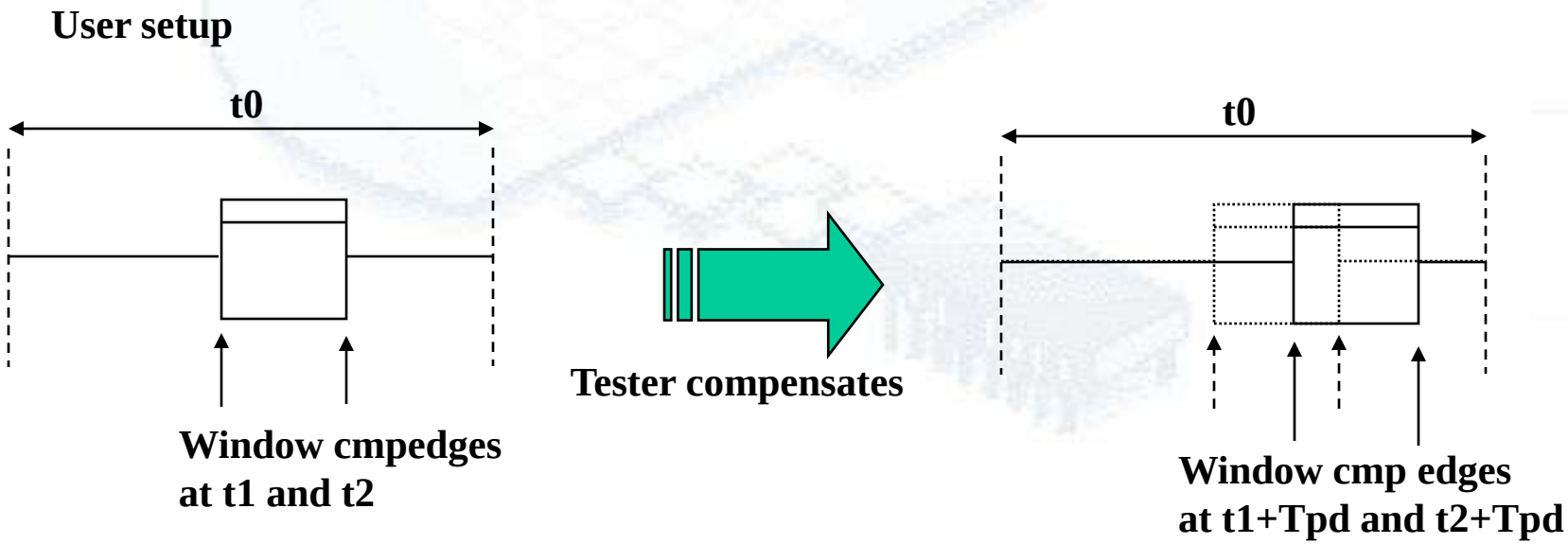
The Tpd of all channels are measured by the tester during TDR calibration. This results are typically stored as a calibration file which the tester uses to compensate for the edge timing setup:



The edge arrives at the DUT pin at programmed edge time.
So, timing setup is DUT referenced and not tester referenced.

PATH DELAY (TDR calibration)

Similarly, the compare edges are also compensated for:



The edge from the DUT arrives at the channel board pin at programmed compare edges time.

Self-Assess Questions

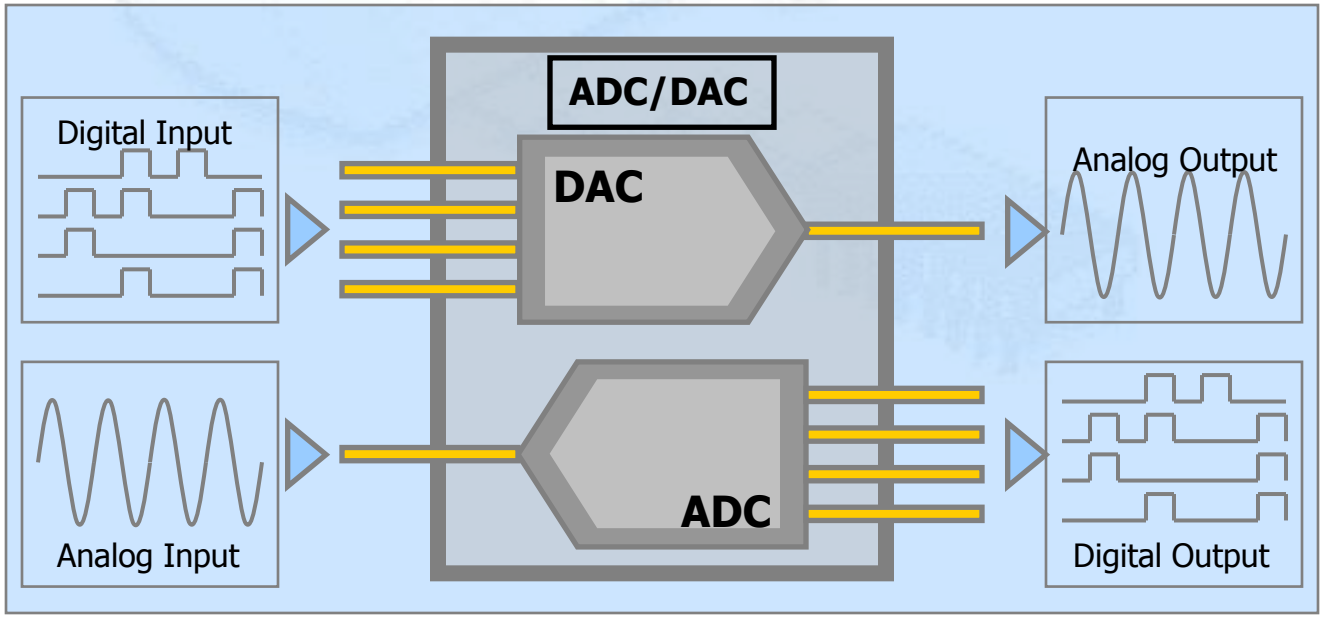
1. Which of this is measured within the same signal (on the same pin)?
   Propagation Delay, Rise time, Period, Duty Cycle

2. Digital Timing is said to be DUT-referenced, and not Tester-reference.
   For this, which of the below needed to be presence (ideally) when timing calibration is performed?
   LoadBoard, Socket, Device, none of these

3. What is the difference between a DC and an AC test?

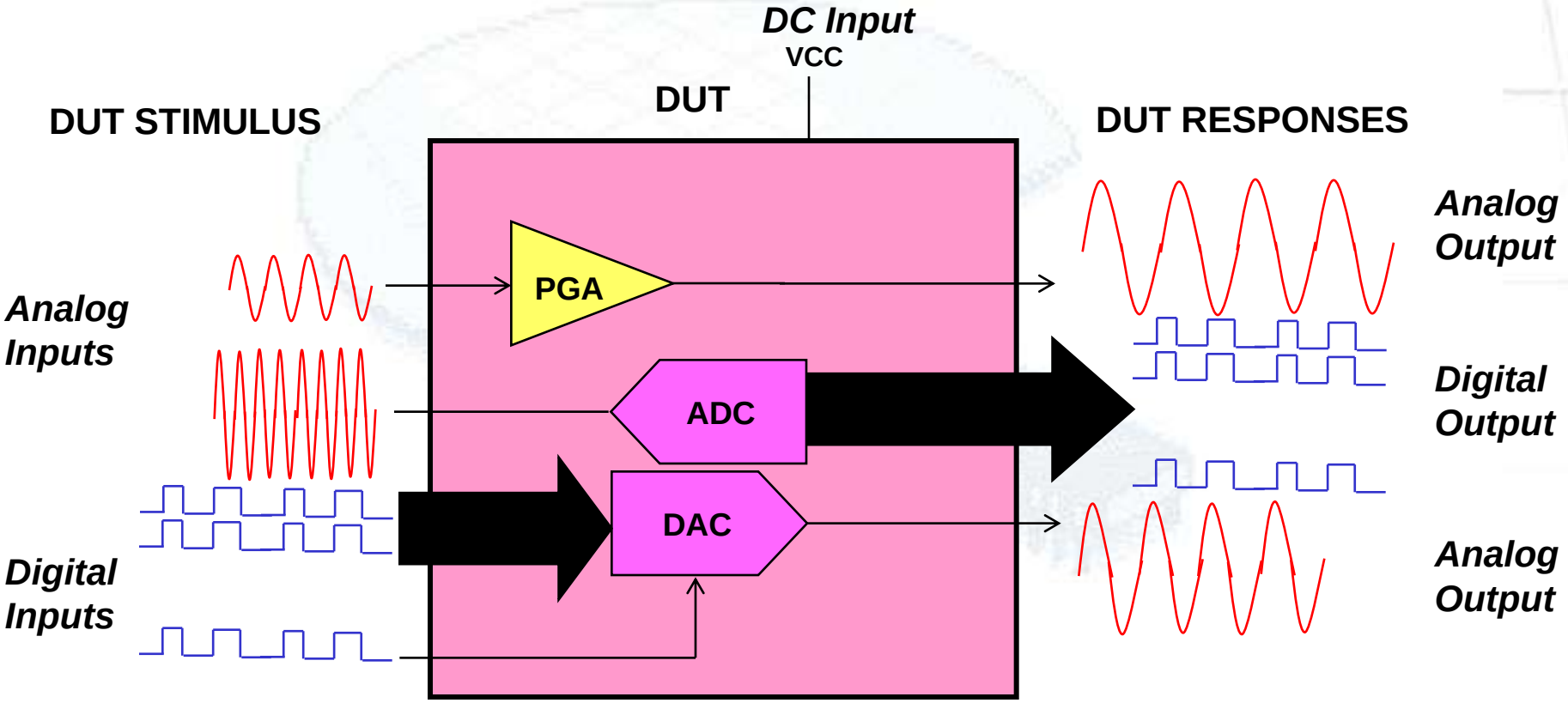
4. One typical timing calibration performed by the ATE is the Path Skew/Deskew. What is the other?

INTRODUCTION TO MIXED SIGNAL TESTING



MIXED SIGNAL TEST

Test signals required by the DUT are analog and digital



Basics – Sampling Theory

Analog Signals

- Signals we use in the real world
- Signal is continuous in both time and amplitude
- Example: our voices

Digital Signals

- To process analog signals in computers, need to convert them to "digital" form
- Signal is discrete in both time and amplitude

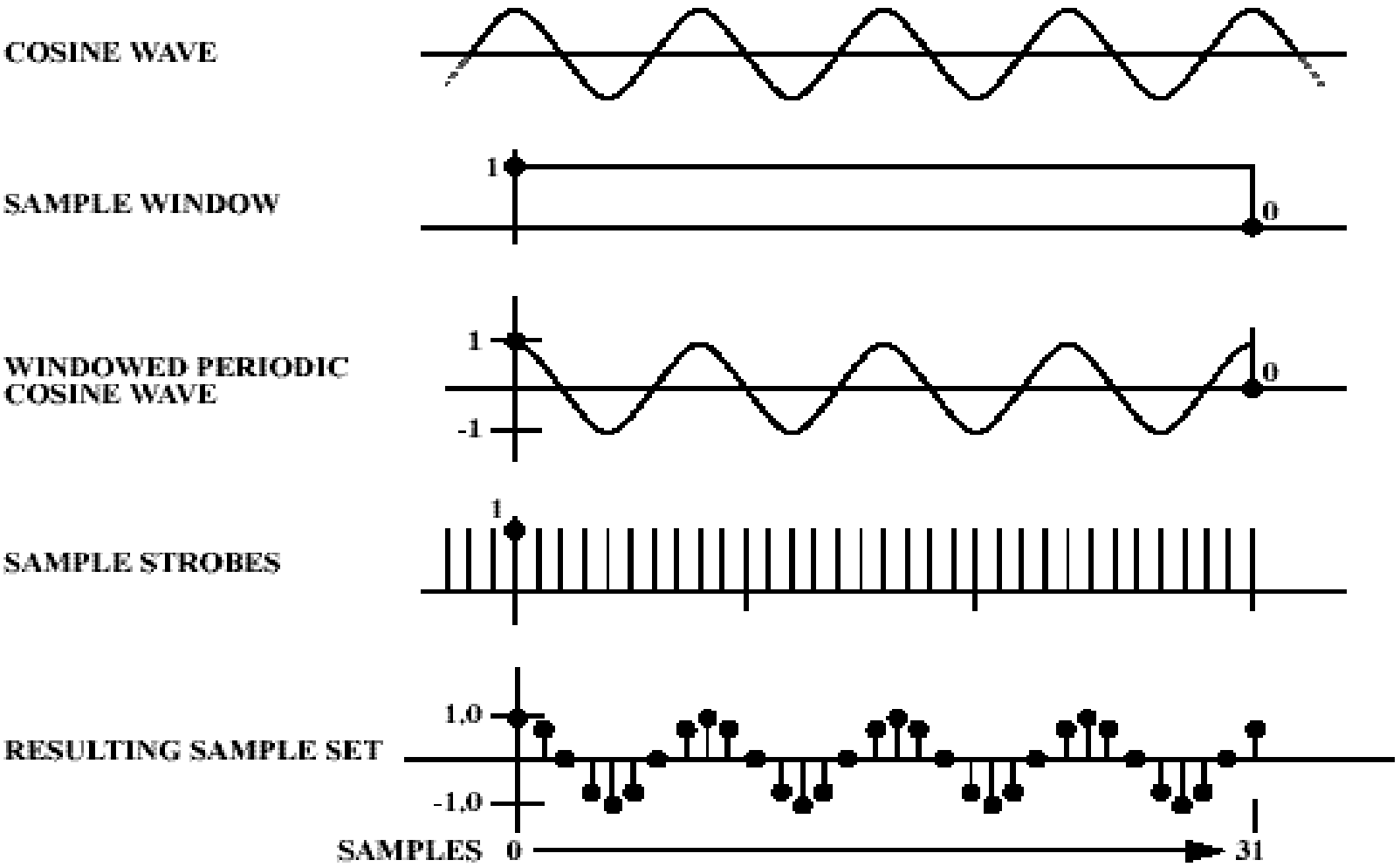
Sample

Each measurement or number

Sample Set

- The series of samples which represent the analog signal
- Also known as the numerical replica of the analog signal.

Basics – Sampling Theory



Basics – Sampling Theory

What is the sampling rate to use to ensure we are preserving the information contained in the signal?

If the signal contains high frequency components, need to sample at a higher rate to avoid losing information that is in the signal.

To be able to recreate a signal from its samples, one must sample at a rate higher than twice the highest frequency of interest, Fi (or frequency of test Ft), contained in the signal.

This is the famous Nyquist Theorem.

$$Fs \geq 2Fi$$

Basics – Sampling Theory

What happens if we sample the signal at a frequency that is lower that the Nyquist rate?

When the signal is converted back into a continuous time signal, it will exhibit a phenomenon called aliasing. Aliasing is the presence of unwanted components in the reconstructed signal.

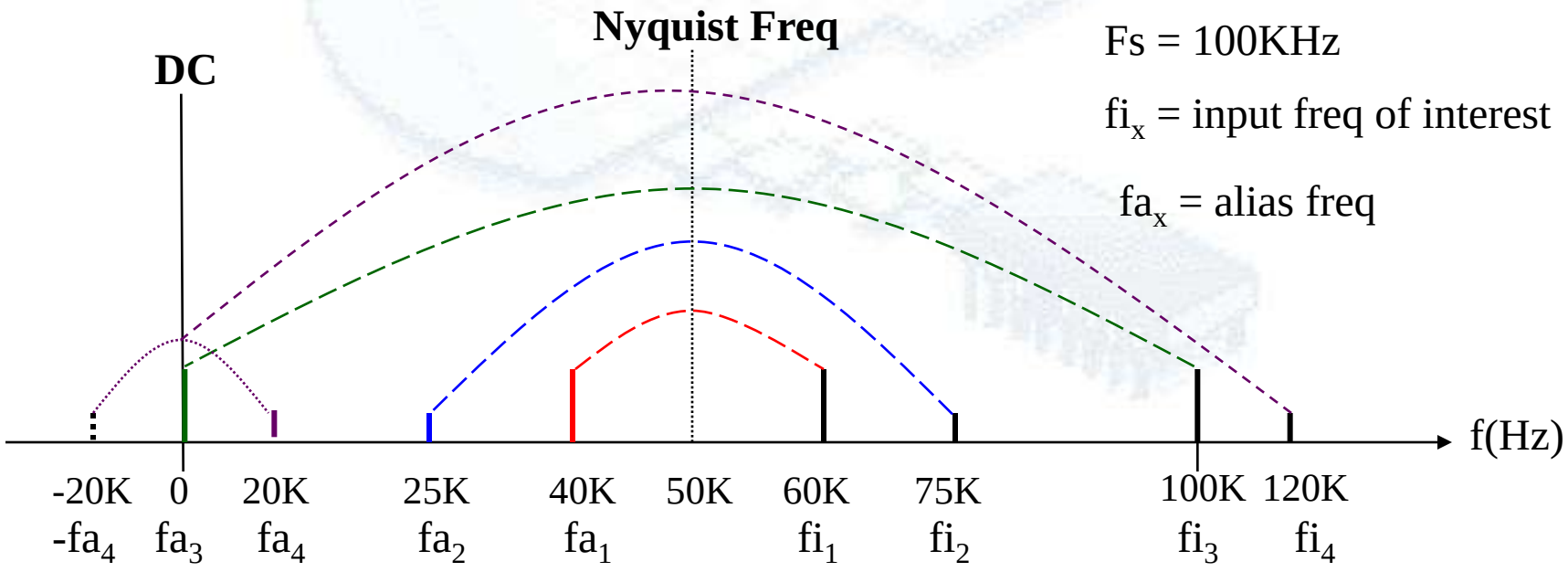
These components were not present when the original signal was sampled.

In addition, some of the frequencies in the original signal may be lost in the reconstructed signal.

Basics – Sampling Theory

Aliasing occurs because signal frequencies can overlap if the sampling frequency is too low.

Frequencies "fold" around half the sampling frequency (Nyquist Frequency).

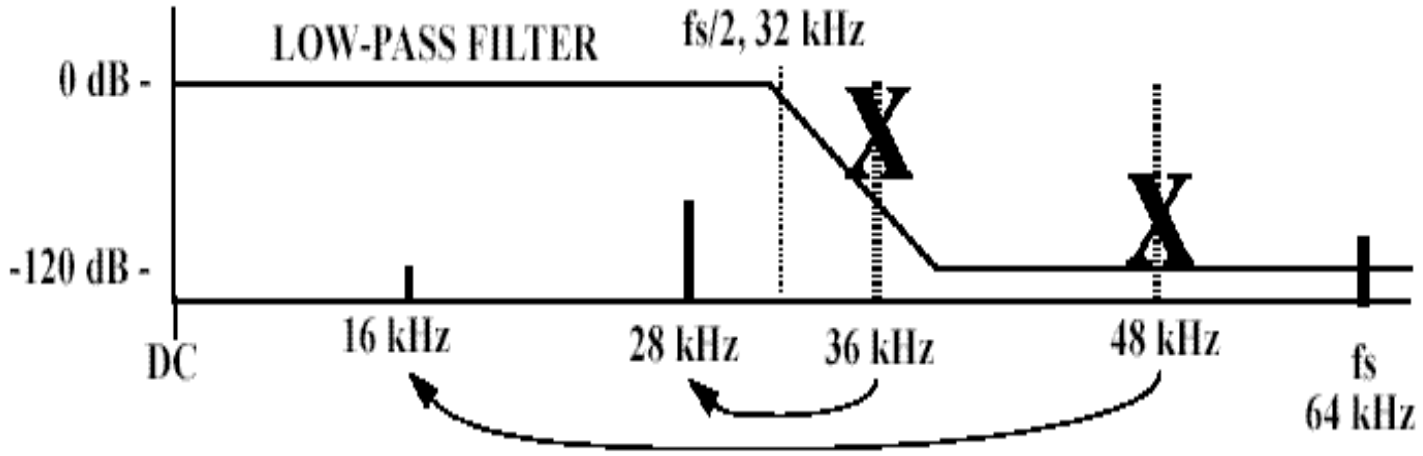


Basics – Sampling Theory

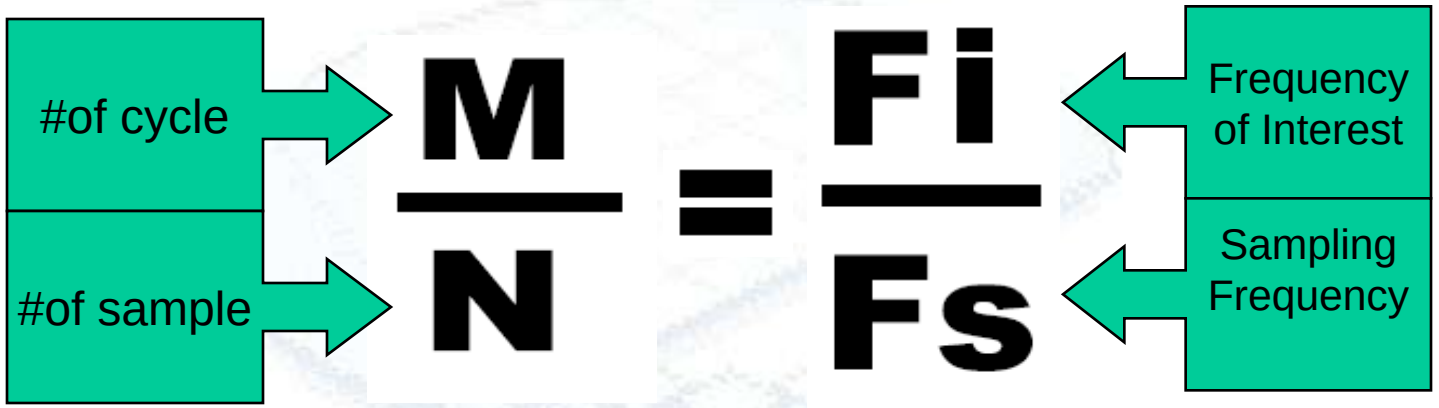
How to minimize aliasing problem?

To minimize aliasing problem, we need to remove frequency components greater than Fs/2 from the signal being digitalized.

Achievable by using an anti-aliasing filter; i.e. a low-pass-filter.



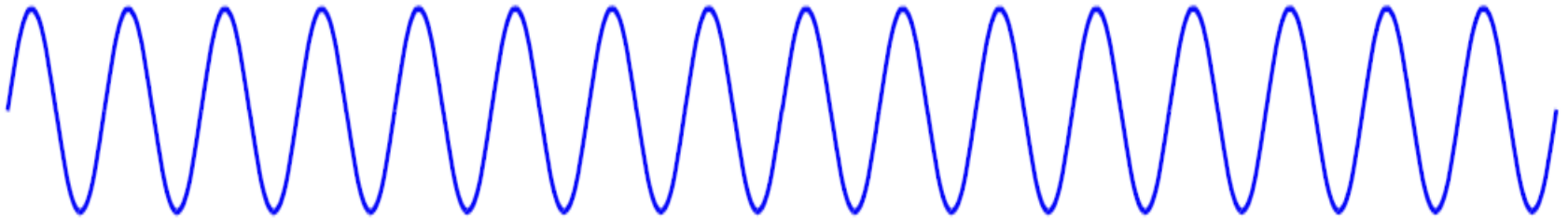
Coherency Formula



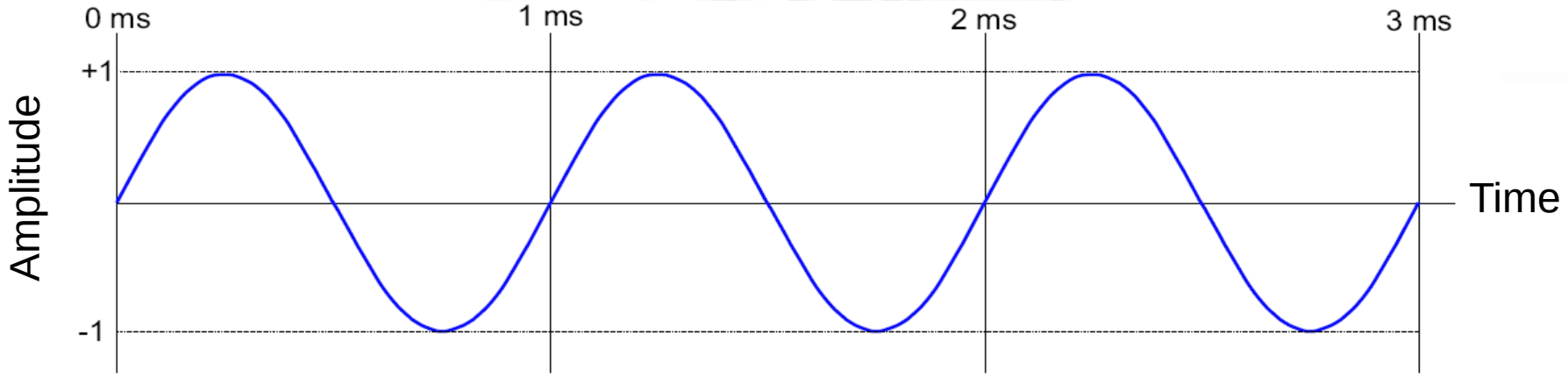
where
Fs = sample frequency
Fi = frequency of interest
N = number of samples
M = number of Fi cycles over which samples are taken

Practical Sampling Theory

1. Let's assume, we have a continuous repeating sinewave with a frequency of 1 kHz.

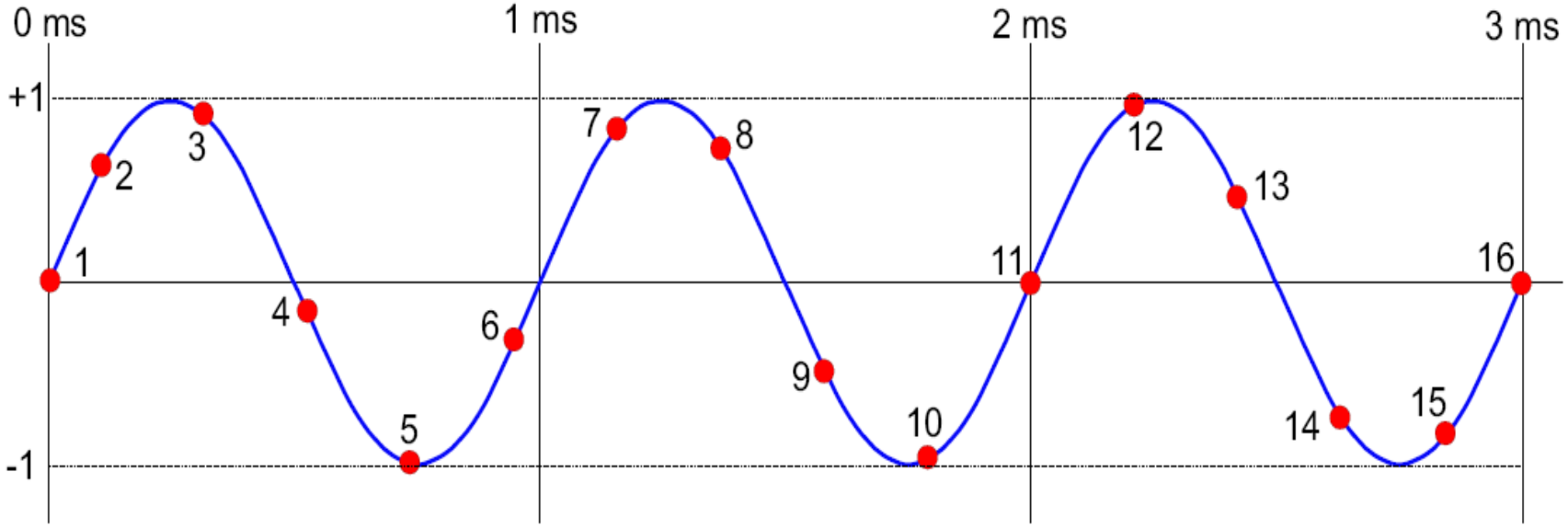


2. We take a **part** of the sinewave, and **scale** it. We are in the Time Domain.



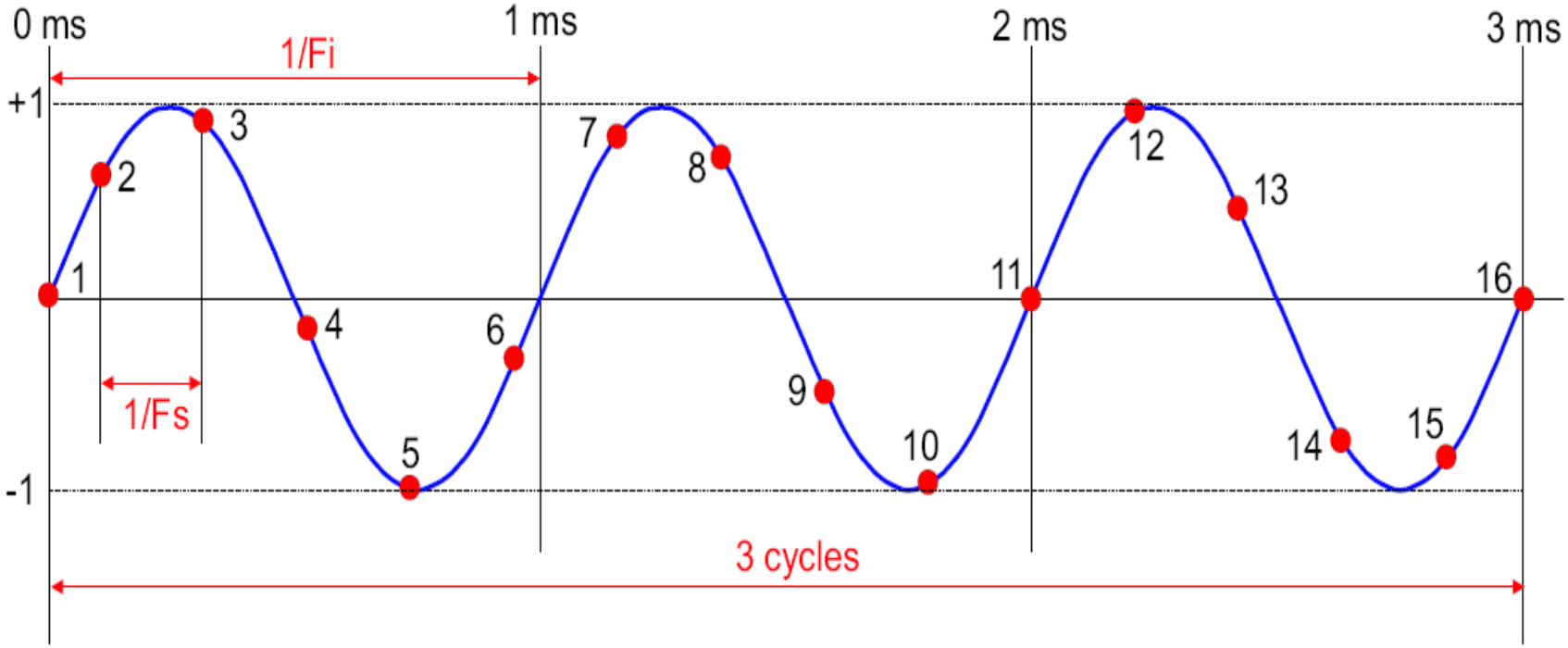
Practical Sampling Theory

3. Next, we take 16 measurements (samples), and store them in an array



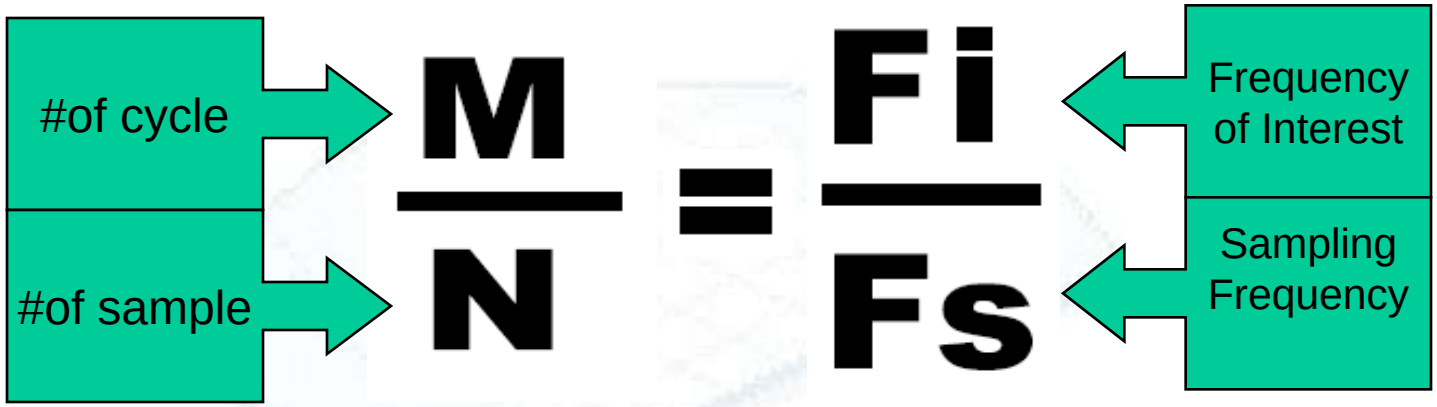

```
float sine_array[16] = {   0.00   /* sample #1  */      -0.46,   /* sample #9  */
                           0.62,   /* sample #2  */      -0.93,   /* sample #10 */
                           0.90,   /* sample #3  */       0.00,   /* sample #11 */
                          -0.15,   /* sample #4  */       0.96,   /* sample #12 */
                          -0.96,   /* sample #5  */       0.45,   /* sample #13 */
                          -0.38,   /* sample #6  */      -0.71,   /* sample #14 */
                           0.82,   /* sample #7  */      -0.80    /* sample #15 */
                           0.71,   /* sample #8  */       0.00    /* sample #16 */  };
```

Practical Sampling Theory



To make calculations for sourcing & capturing, we use the following:
Fi the frequency of interest = 1khz
Fs the sample frequency = ??
M the number of cycles = 3
N the number of samples =16

Practical Sampling Theory



In our example: fi = 1kHz
M = 3
N = 16

so: $\frac{Fi}{Fs} = \frac{M}{N} \rightarrow \frac{1\ kHz}{Fs} = \frac{3}{16} \rightarrow Fs =$ 5.333kHz

Coherent Sampling

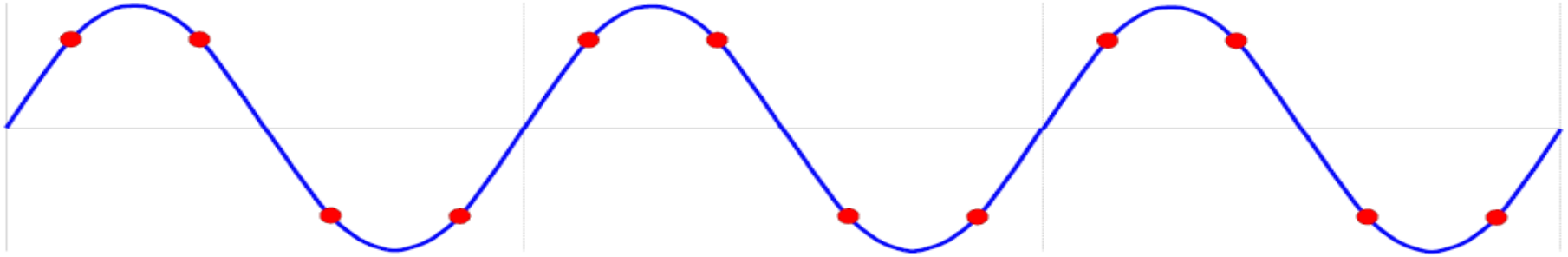
Considerations in using variables in the balanced ratio

Fi, Fs, M, N

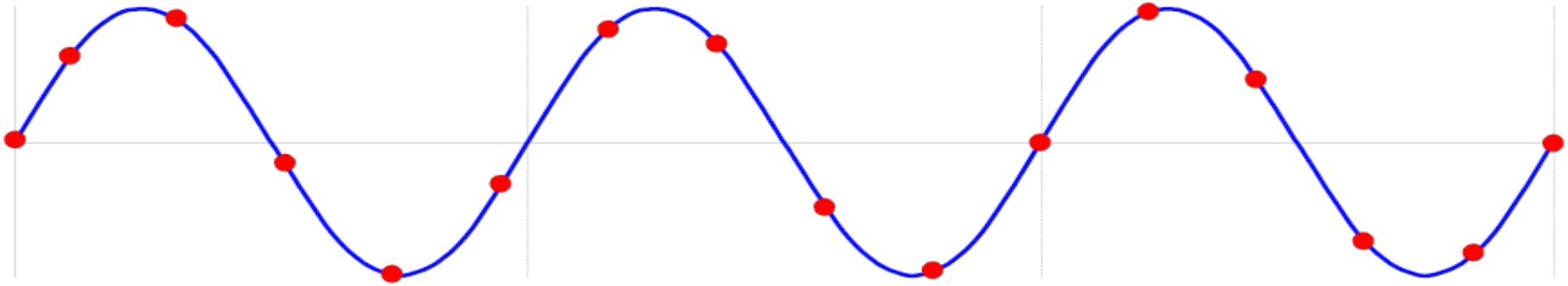
- Increasing M and/or N will increase accuracy and test time
- M needs to be a whole number to have a coherent waveform (a whole number of cycles or complete/full cycles)
- N has to be a whole number because there is no such thing as half a sample
- N needs to be a power of 2 to ensure you can use a Fast Fourier Transform (FFT)
- M and N must be "mutually prime" otherwise you waste test time because in each cycle you sample the same points over and over.
- Minimum Fs = >2*Fi (Nyquist Theorm)

Coherent Sampling

Why M and N must be "Mutually Prime"



Above M=3 and N= 12 so they are not mutually prime or lowest common denominator. In every cycle, samples are taken at the same position, there is no new information.



In this case M=3 and N=16, so they are mutually prime and every sample is discrete, that is it gives unique information, sampling a different point in time.

Example

If you want to generate a 10 MHz sinewave that repeats after every 256 samples, you must select a sampling frequency at least twice the frequency of the desired Fi.

Choosing a Fs of 8 x Fi gives 80 MHz, so that at first pass the equation becomes

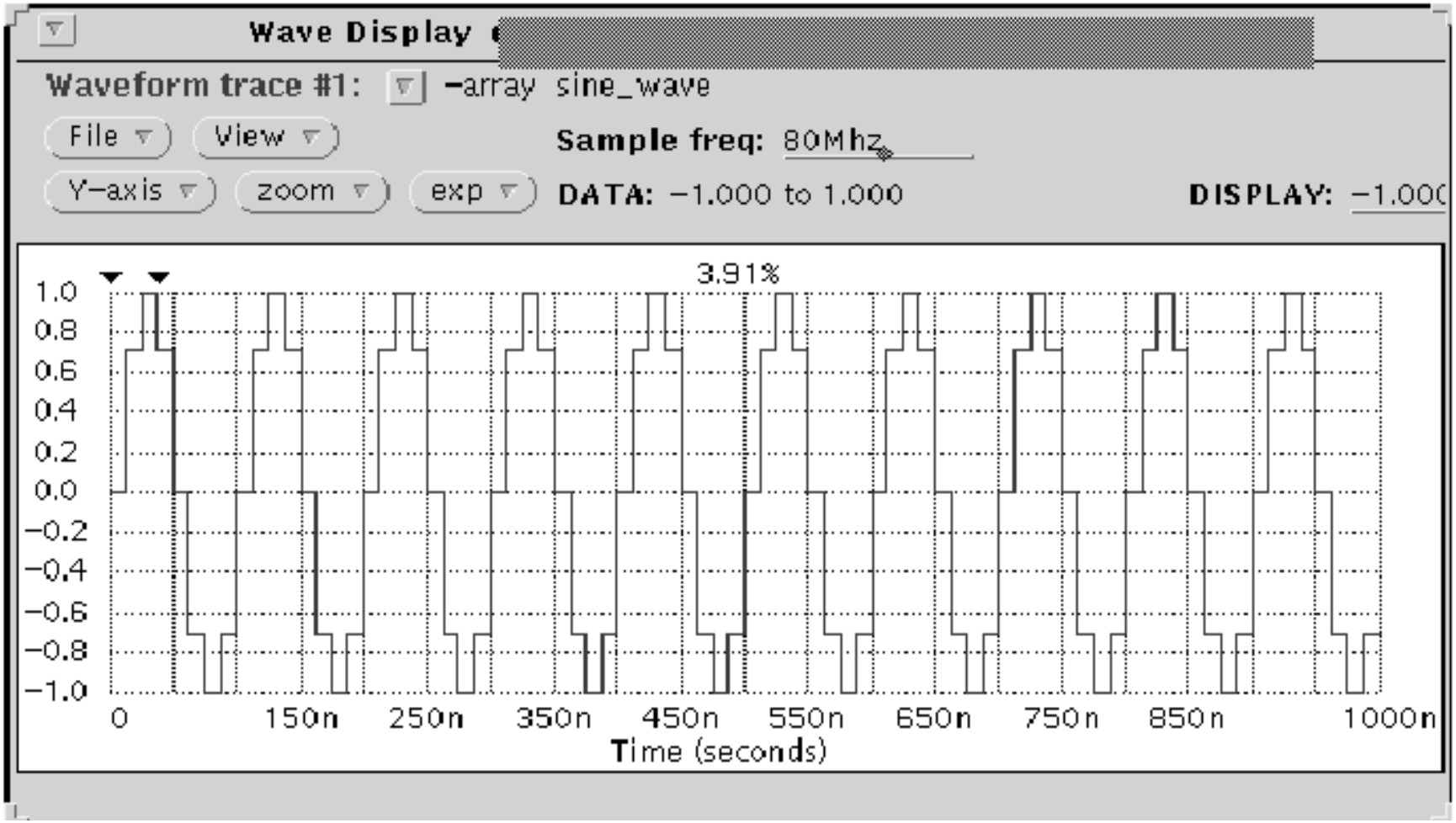
$$N/M = 256/M = 80\ MHz/10\ MHz \quad (2)$$

$$M = 256*(10\ MHz/80\ MHz) = 32 \quad (3)$$

You can see from equation (3) that M satisfies the requirement of being an integer number of cycles, but it places the samples in exactly the same position on the sinewave for all 32 cycles. (Not mutually prime)

For converter testing this means the same eight codes are tested over the sample window as shown below.

Basics – Sampling Theory



Periodic Sample Generation, but not mutually prime

Revised 8/8/2007

Basics – Sampling Theory

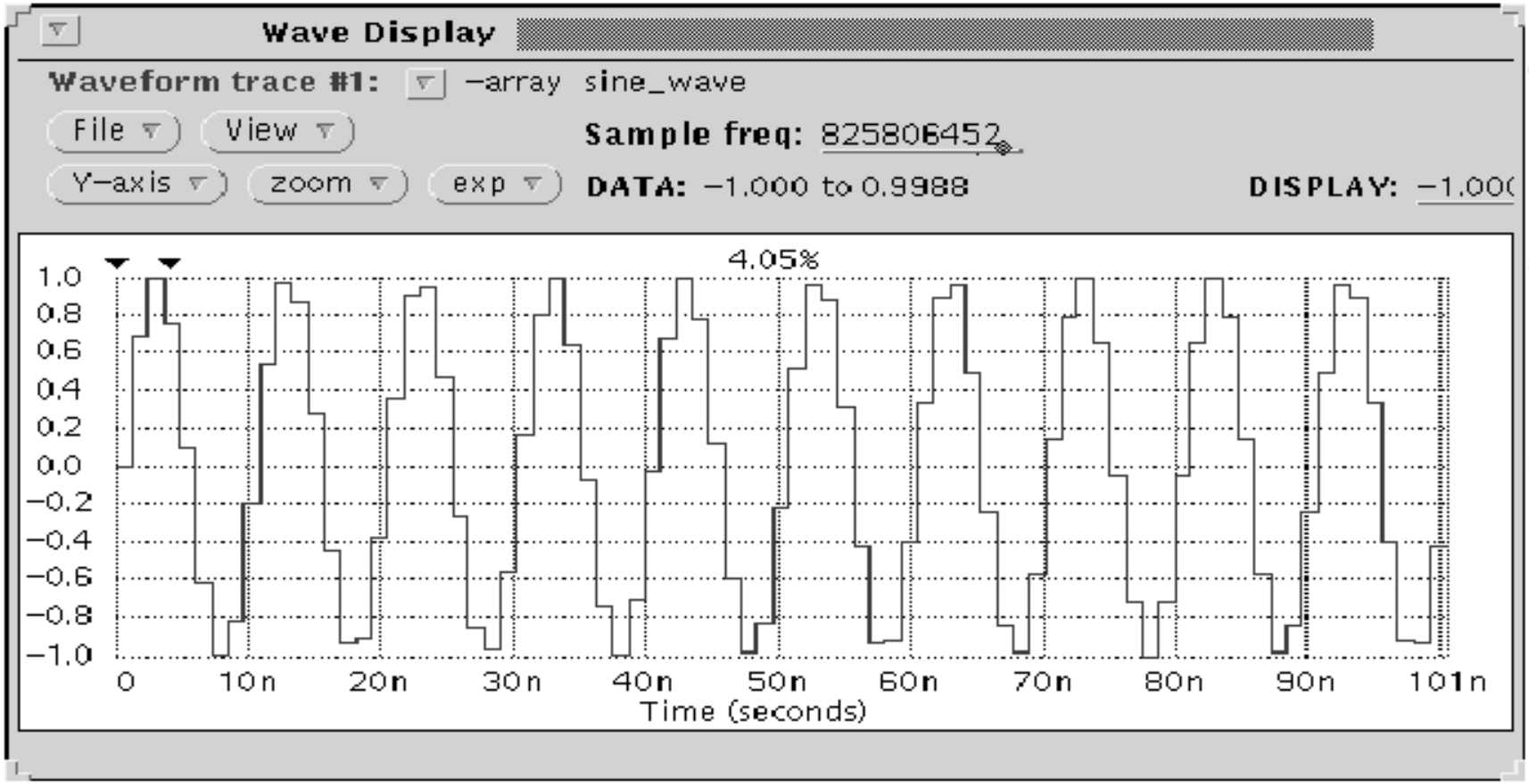
A better approach is to uniquely distribute the 256 samples across the windows. To do this, use an integer prime number for M close to the desired value that still satisfies the other conditions.

In this case, use M=31 so equation (2) becomes

$$N/M = 256/31 = Fs/Fi = 82.58064516 \text{ MHz} / 10 \text{ MHz} \quad (4)$$

Basics – Sampling Theory

A better approach is to uniquely distribute the 256 samples across the sample window as shown below.



Basics – Sampling Theory

Frequency Resolution (Fres), resolution of the spectrum

$$Fres = Fs/N \qquad (5)$$

Acquisition Time (UTP), time required to take all samples

$$Tacq = 1/Fres$$

In equation (5), the Fres = Fs/N = 82.5 MHz/256 = 322.265 kHz.

Basics – Sampling Theory

Why sample coherently?

When digitizing a waveform, coherent sampling eliminates the need for any time windowing by guaranteeing that the sample set contains a complete, periodic waveform representation.

FFT output from a set of coherent samples puts the relevant information about the fundamental and harmonics into specific, well defined frequency ranges, called bins.

When generating a waveform, there is no leakage because coherent sampling guarantees that there will be exactly a complete set of samples for one or more signal cycles.

Basics – Sampling Theory

What happens if we do not have a complete sample set?

If the time sample set does not form a complete set, leakage occurs.

Discontinuity occurs where 2 sample sets join, causing a sharp edge within a sinusoid.

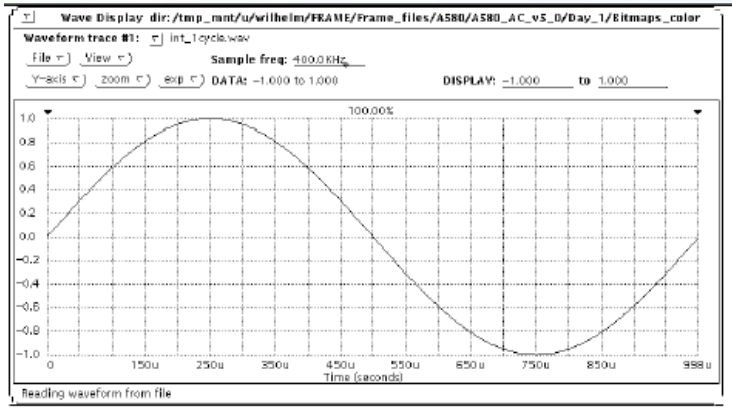
A sharp edge in time has high frequency components.

To minimize the effects of leakage, use time window functions.Examples of window function: Hann, Hamming and Blackman

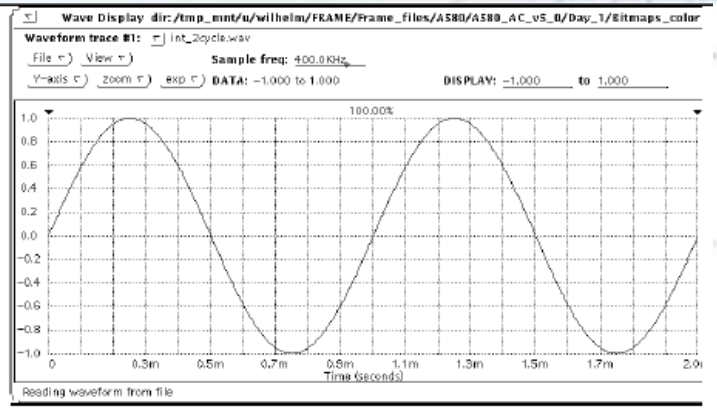
To eliminate the effects of leakage, use coherent sample set.

What does the FFT see?

PERIODIC SAMPLE SET

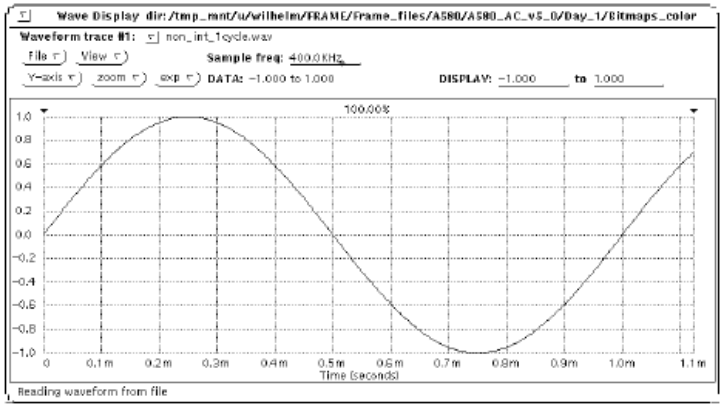


SINGLE

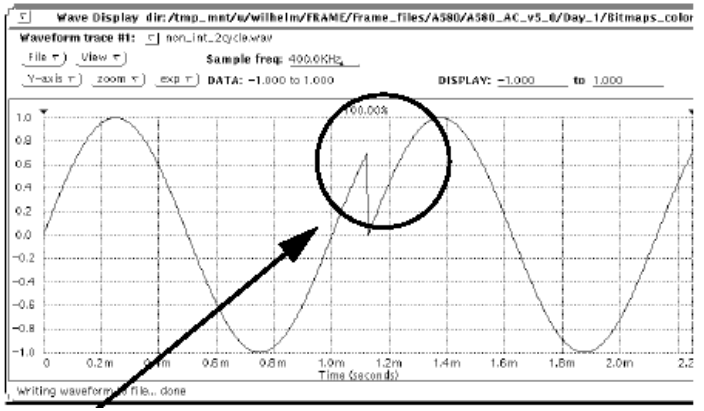


REPEATED

NONPERIODIC SAMPLE SET



SINGLE



REPEATED

DISCONTINUITY

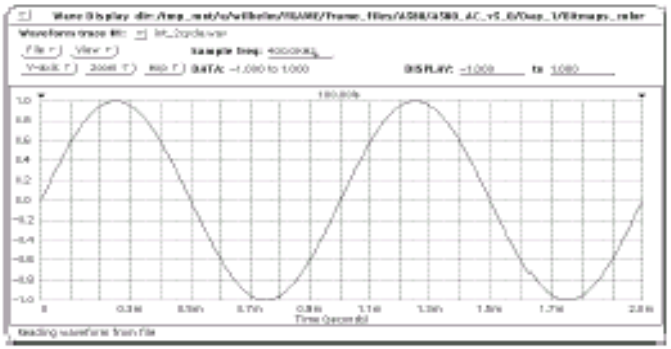
Basics – FFT

Coherent capture is a prerequisite to successful FFT operations.
Non integer period capture will cause spectral smearing:

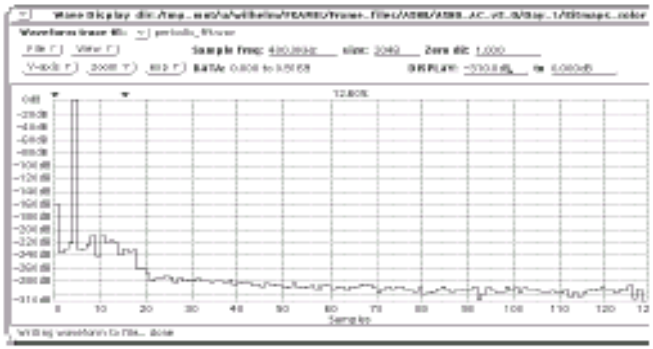
Fs/Fi=N/M

M=2

TIME DOMAIN

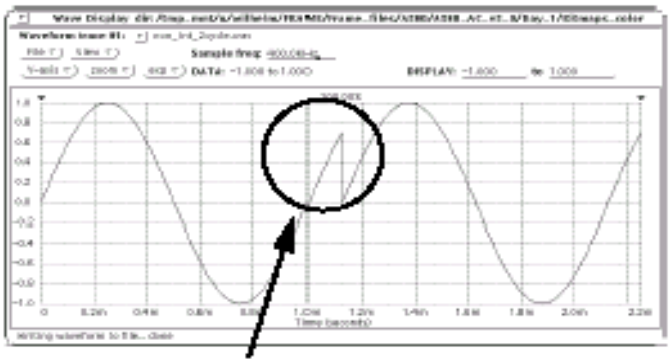


FREQUENCY DOMAIN

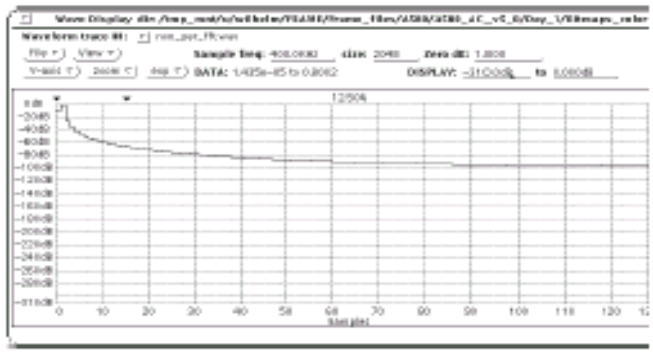


M=1.25

TIME DOMAIN



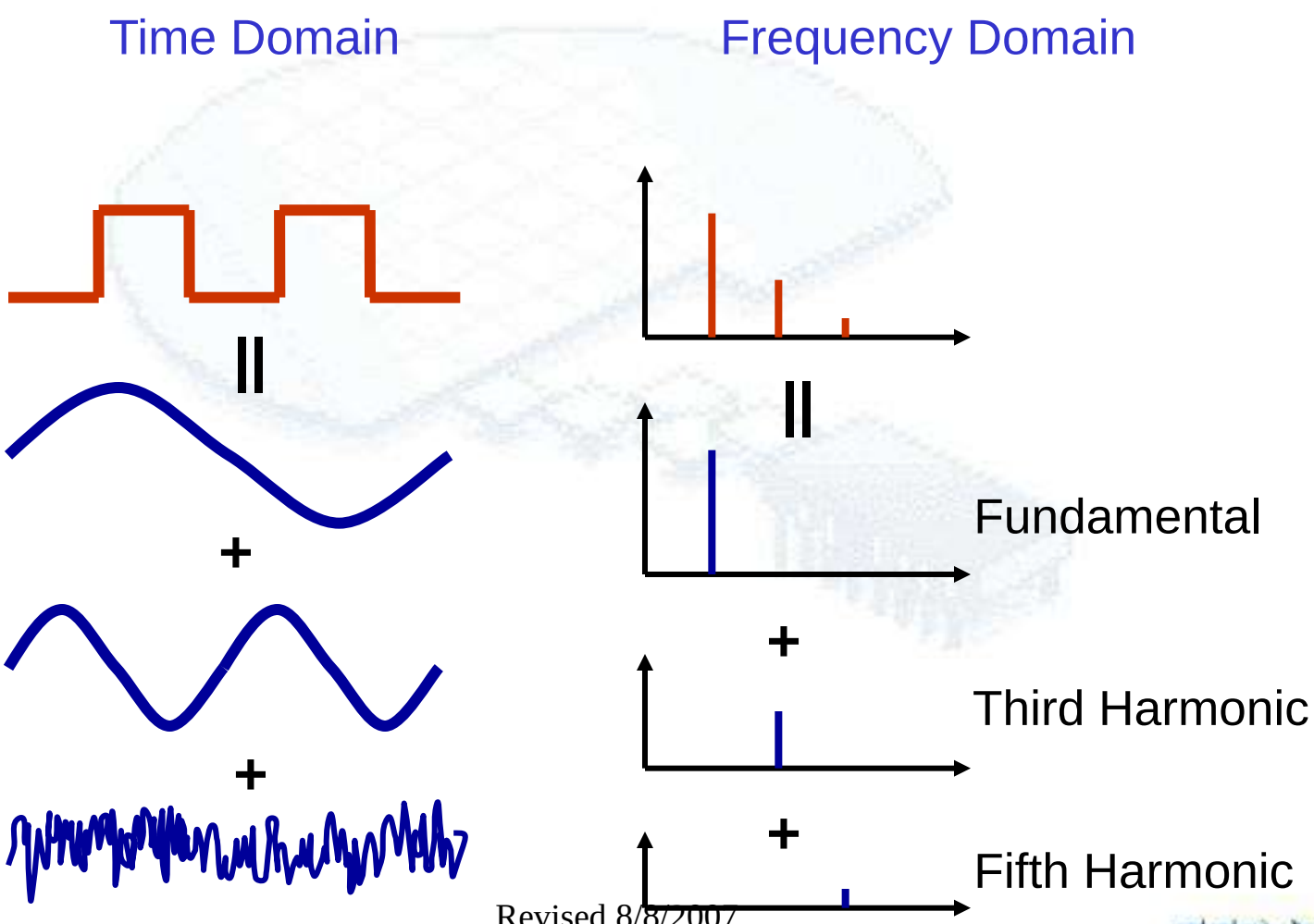
FREQUENCY DOMAIN



DISCONTINUITY CAUSES WIDE BAND NOISE (SMEARING)

Revised 8/8/2007

Fundamental of FFT



Basics – FFT

- **Fourier Transform (FT)**
  - Continuous-time signals – possible only theoretically.
  - Cannot be implemented using a computer.

- **Discrete Fourier Transform (DFT)**
  - Sampled signals – finite number of samples.
  - Extensive math – time consuming – n^2 mathematical iterations.
    - Ex: 4,000 samples ~ 16,000,000 iterations

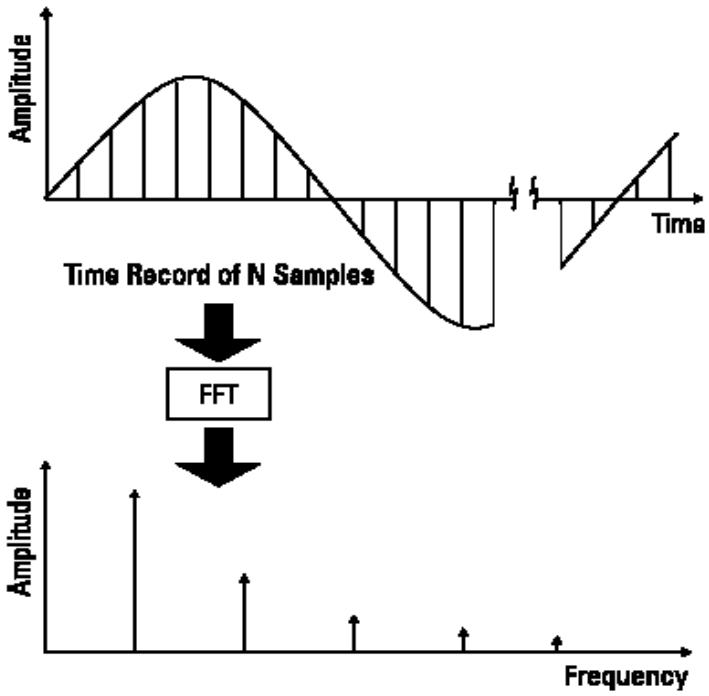
- **Fast Fourier Transform (FFT)**
  - Sampled signals – 2^n number of samples. Ex: 4, 16, 32, ...
  - Simplified math – $n\log_2 n$ mathematical iterations.
    - Ex: 4,096 samples ~ 49,152 iterations

Basics – FFT

The Fast Fourier Transform (FFT) is an algorithm for transforming data from the time domain to the frequency domain.

A time-record is defined to be N (sample size) consecutive, equally spaced samples of the input.

N is restricted to be a multiple of 2 as it makes our transform algorithm simpler and much faste



Basics – FFT

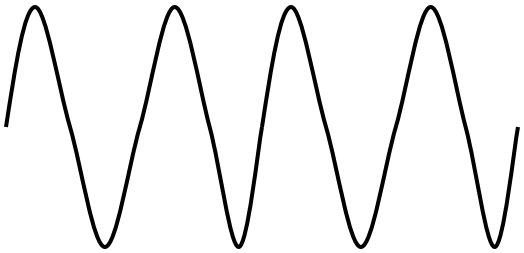
FFT assumes periodicity in all cases.

FFT is a linear transform whereby two or more waveforms can be summed in the time domain to give a third function. Likewise, the frequency domain of this new function is the sum of the frequency domains of the original functions.

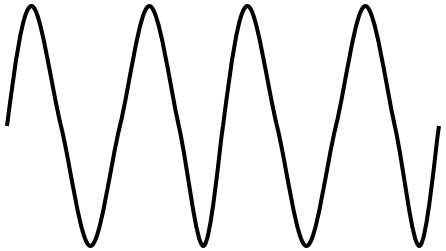
Any multi-tone signal is actually made up of multiple single-tone signals.

Basics – FFT

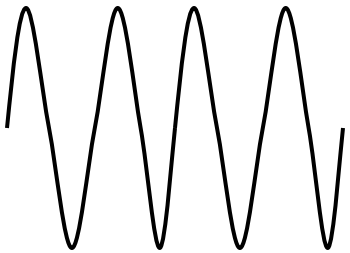
FI_M1 = 8,750 Hz (M = 35)



FI_M2 = 10,750Hz (M = 43)



FI_M3 = 12,750Hz (M = 51)



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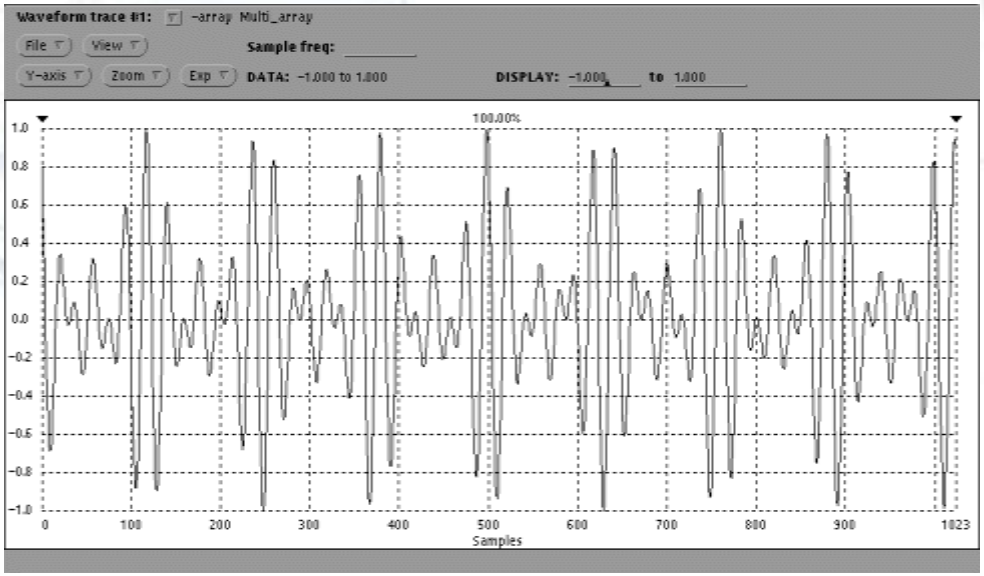
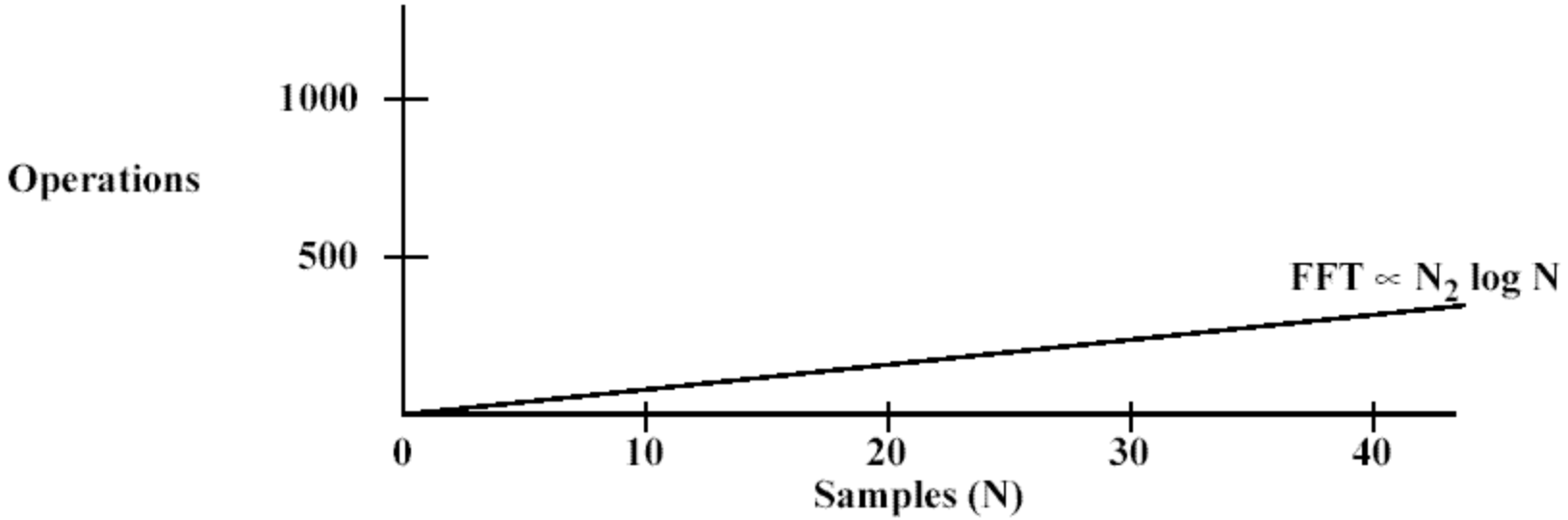


Basics – FFT

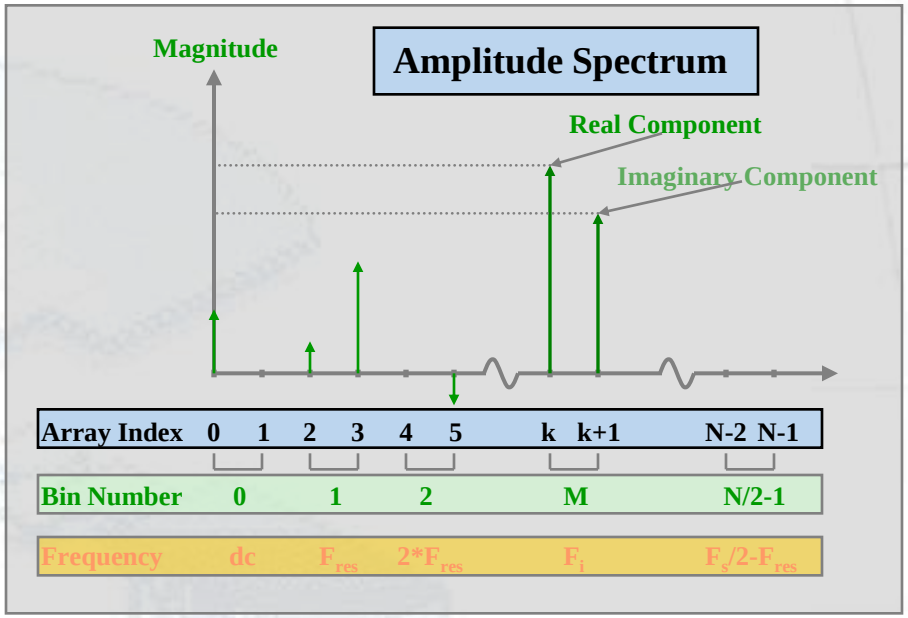
Test time increases with increasing sampling size as the number of operations required for computation increases.

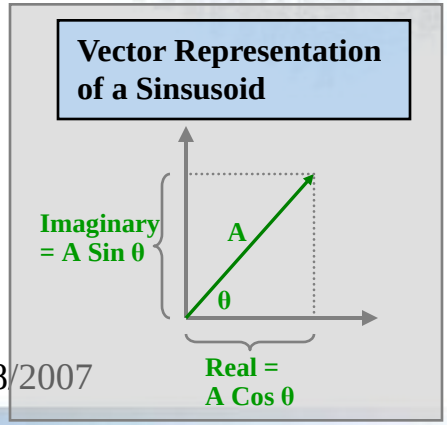


The output of FFT is usually in rectangular coordinates.
Need to convert to polar form to obtain magnitude and phase information.

Basics – FFT (Amplitude Spectrum)

- For N (power of 2) time domain samples, there will be N frequency domain values.
- The N values are grouped in pairs called **bins** (0,1 -> bin 0; 2,3 -> bin 1; 4,5 -> bin 2; ...) that represent one frequency component (magnitude and phase).
- The two values are a real and imaginary component that represent a sinusoidal component with a given phase and amplitude





$F_i / F_s = M / N$

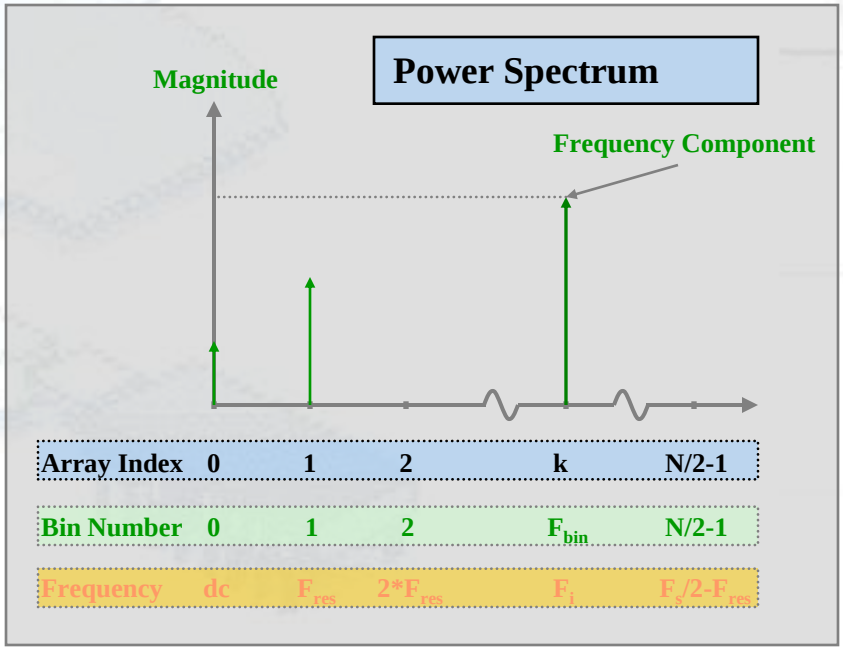
$F_{res} = F_s / N$

$M = F_i \times N / F_s$

$= F_i / F_{res}$

Basics – FFT (Power Spectrum)

- For **N** time-domain signal samples
- There are **N** frequency-domain signal values
- There are **N/2** frequency-domain – Power Spectrum values



Frequency Domain Signal Definitions

Frequency Bin	The frequency spectrum contains signal amplitudes at discrete frequencies normally called frequency bins.
DC Component	The first frequency bin resulting from the FFT is the DC component of the signal.
Fundamental	This is the frequency of interest. The input signal to the A/D.
Spectrum	The entire array of frequencies represented by the FFT.
Harmonics	Odd and even multiples of the fundamental signal.
Noise	The frequency components represented in a given bandwidth other than the DC component, fundamental, and harmonics.
RMS	Root Mean Squared.

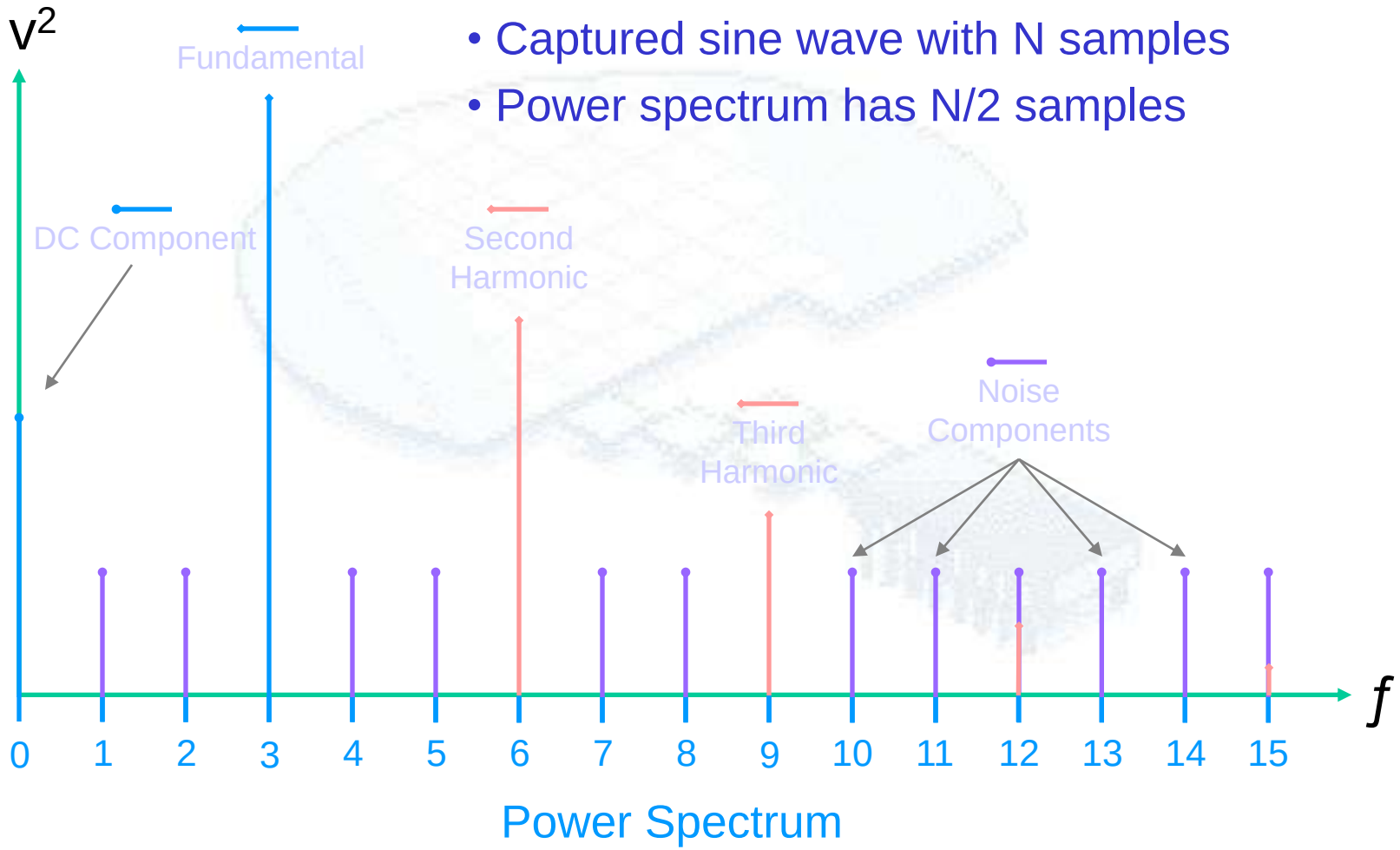
Frequency Analysis

Common Frequency Analysis Algorithms

- Signal To Noise Ratio (SNR)
- Total Harmonic Distortion (THD)
- Signal to Noise and Distortion (SINAD)
- Spurious Free Dynamic Range (SFDR)

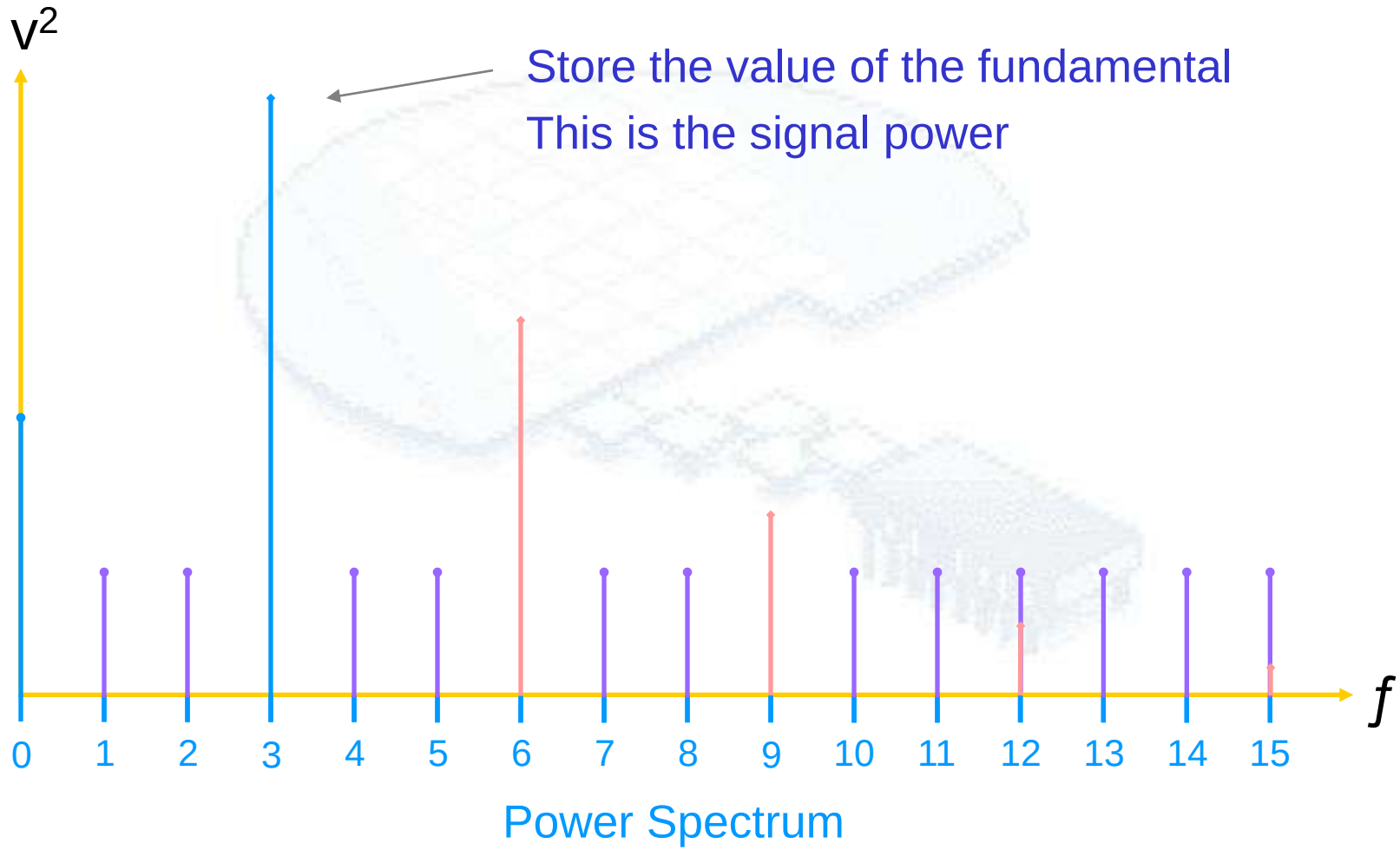
What are the Spectral Components?

- Captured sine wave with N samples
- Power spectrum has N/2 samples



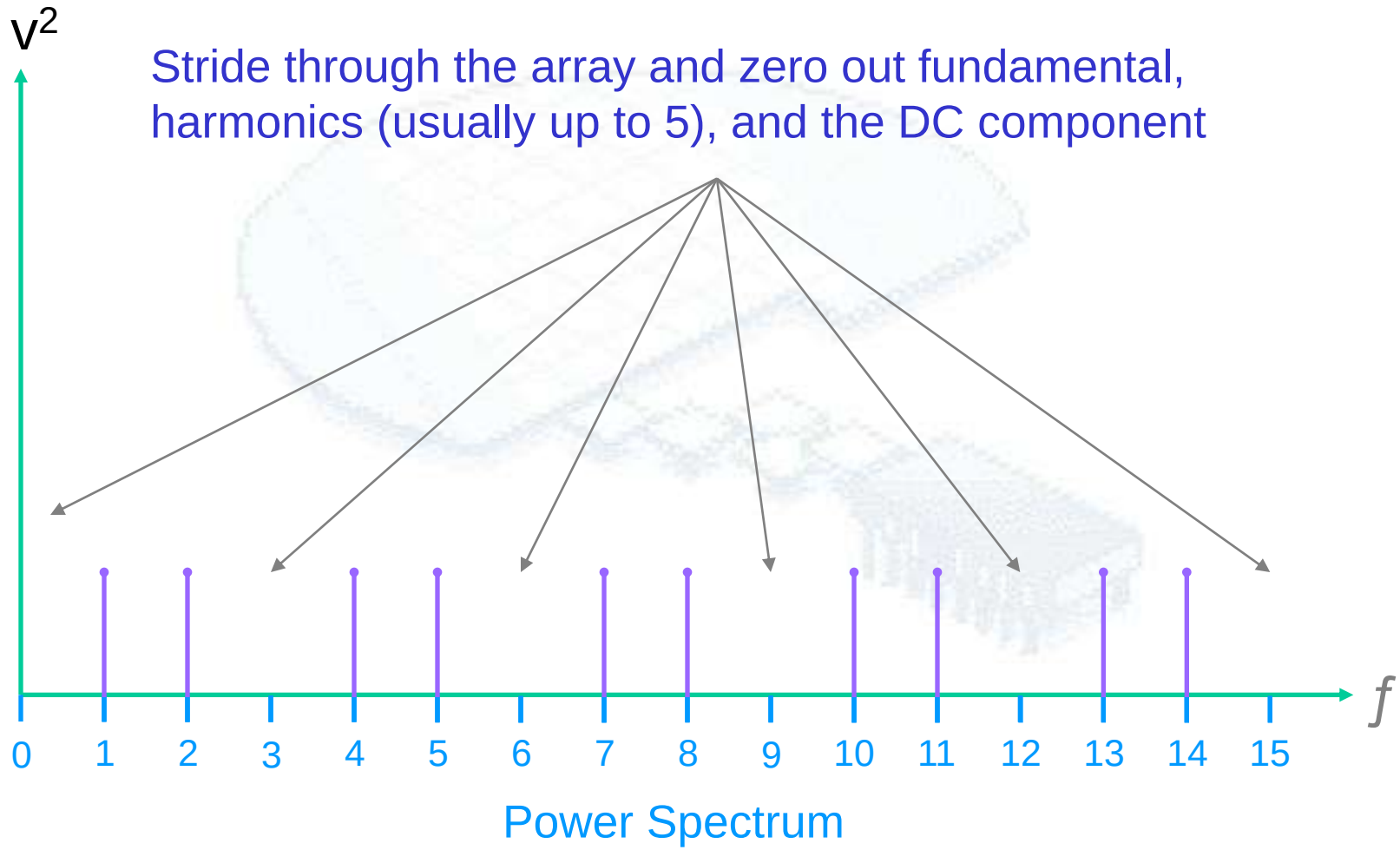
Power Spectrum

Signal to Noise Ratio (SNR)

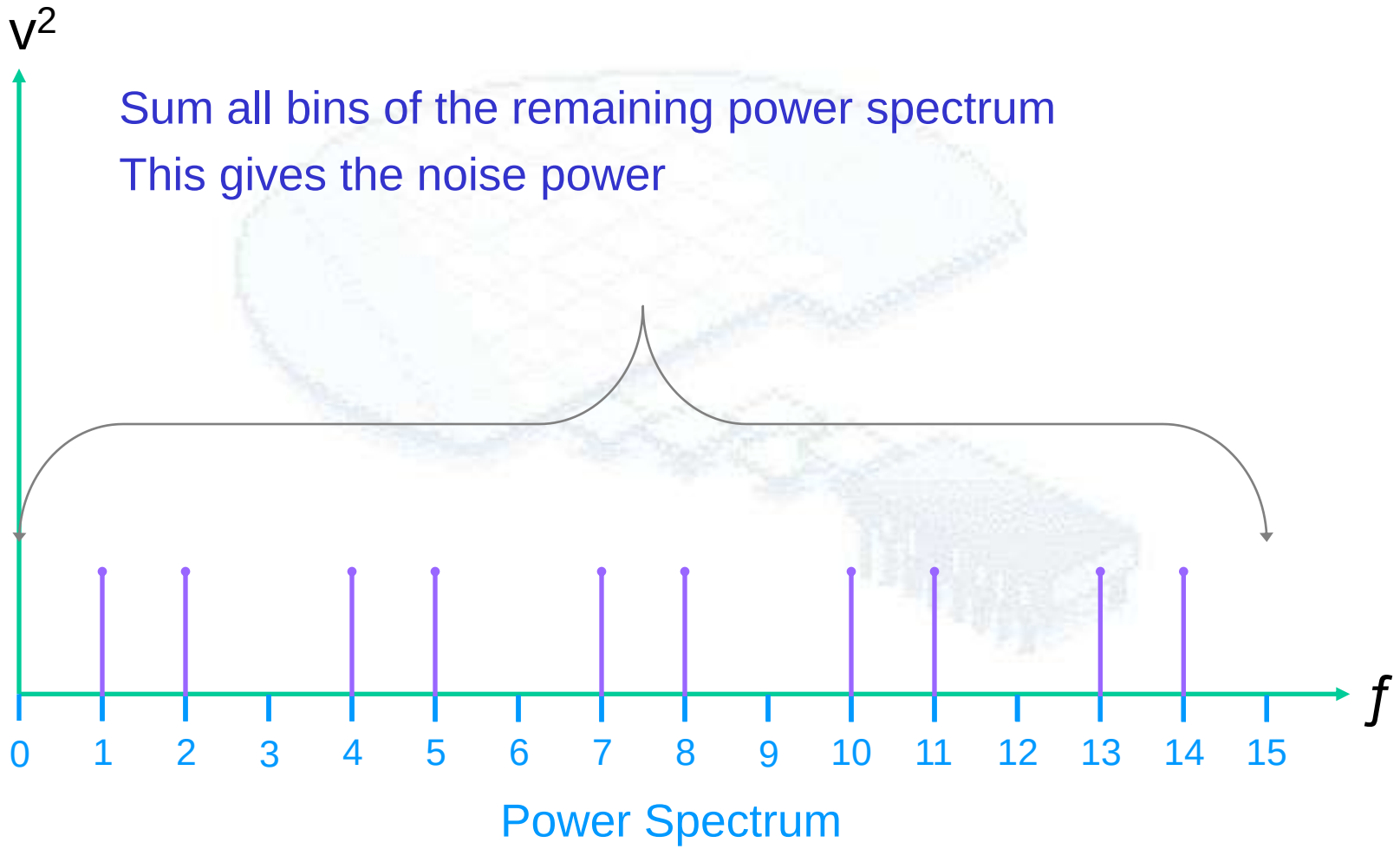


Power Spectrum

Signal to Noise Ratio (SNR)



Signal to Noise Ratio (SNR)

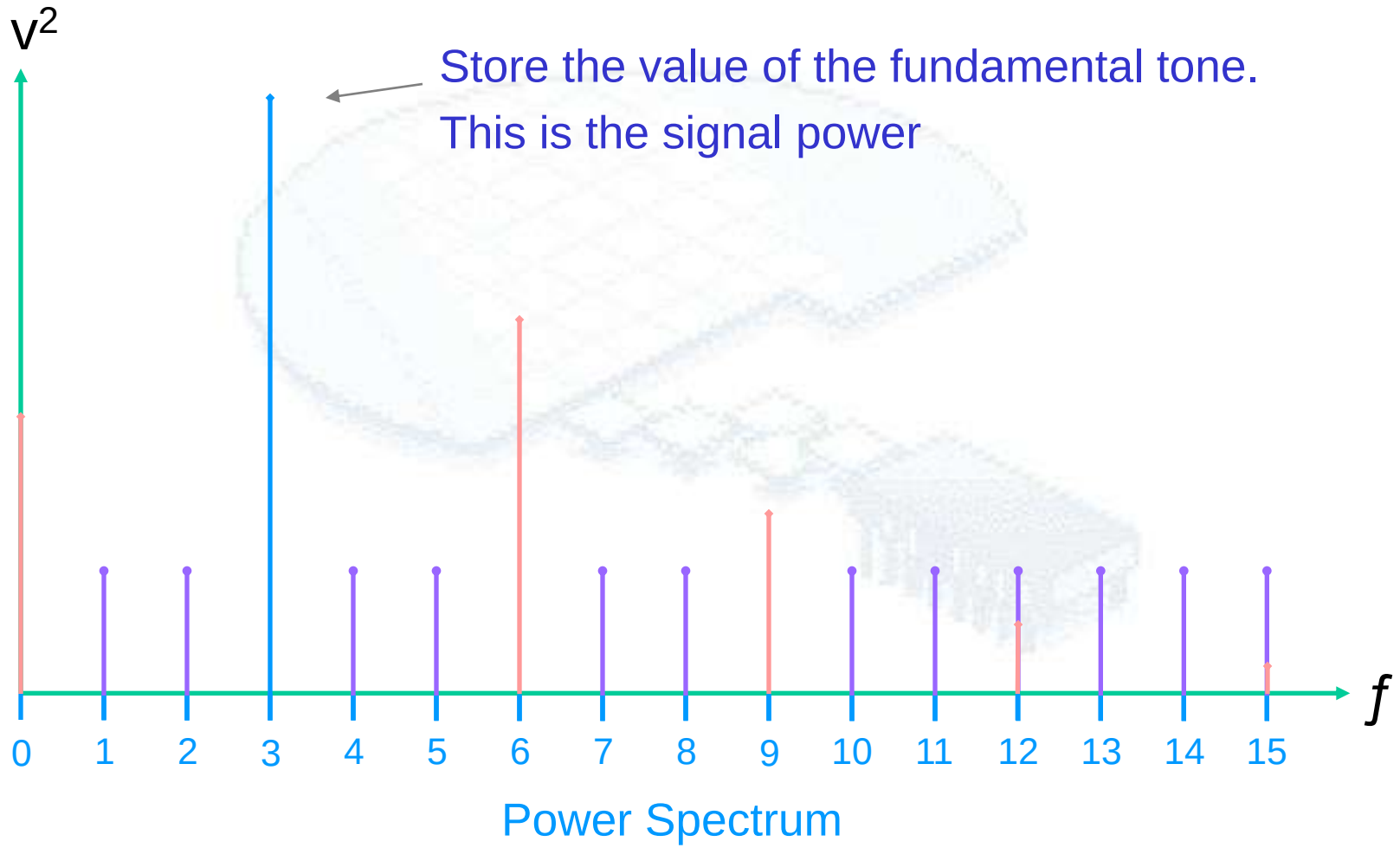


Signal to Noise Ratio (SNR)

- Expressed in decibels (dB)
- The signal to noise ratio is a positive value (assuming the fundamental power is greater than the noise power)

$$SNR_{dB} = 10 \log_{10} \left[\frac{\text{Fundamental}}{\text{Noise Power}} \right]$$

Total Harmonic Distortion (THD)

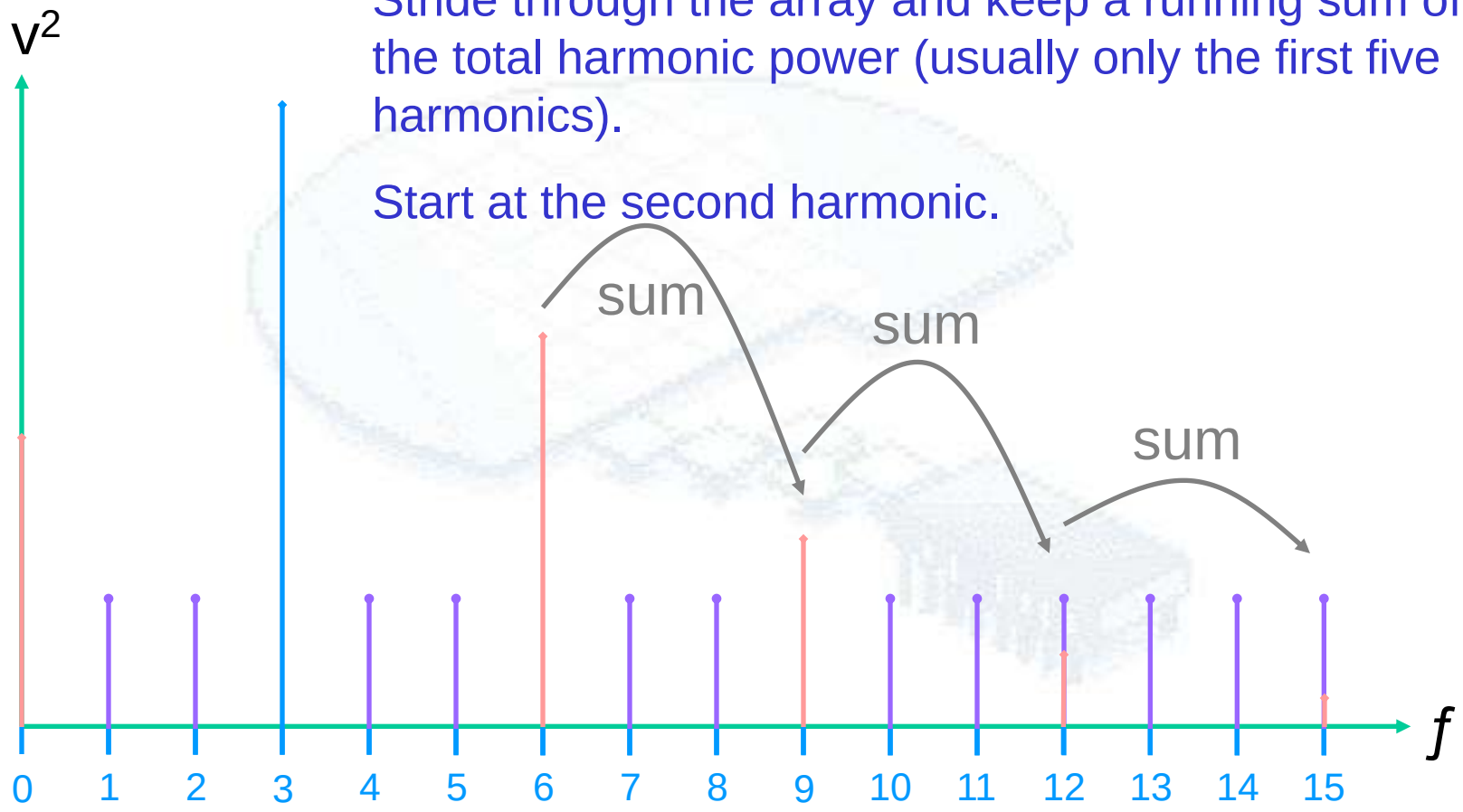


Revised 8/8/2007

Total Harmonic Distortion (THD)

Stride through the array and keep a running sum of the total harmonic power (usually only the first five harmonics).

Start at the second harmonic.



Power Spectrum

Total Harmonic Distortion (THD)

- Expressed in decibels (dB)
- The THD is a negative value (assuming the fundamental power is greater than the noise power)

$$THD_{dB} = 10 \log_{10} \left[\frac{\text{Harmonic Power}}{\text{Fundamental}} \right]$$

Signal to Noise and Distortion (SINAD)

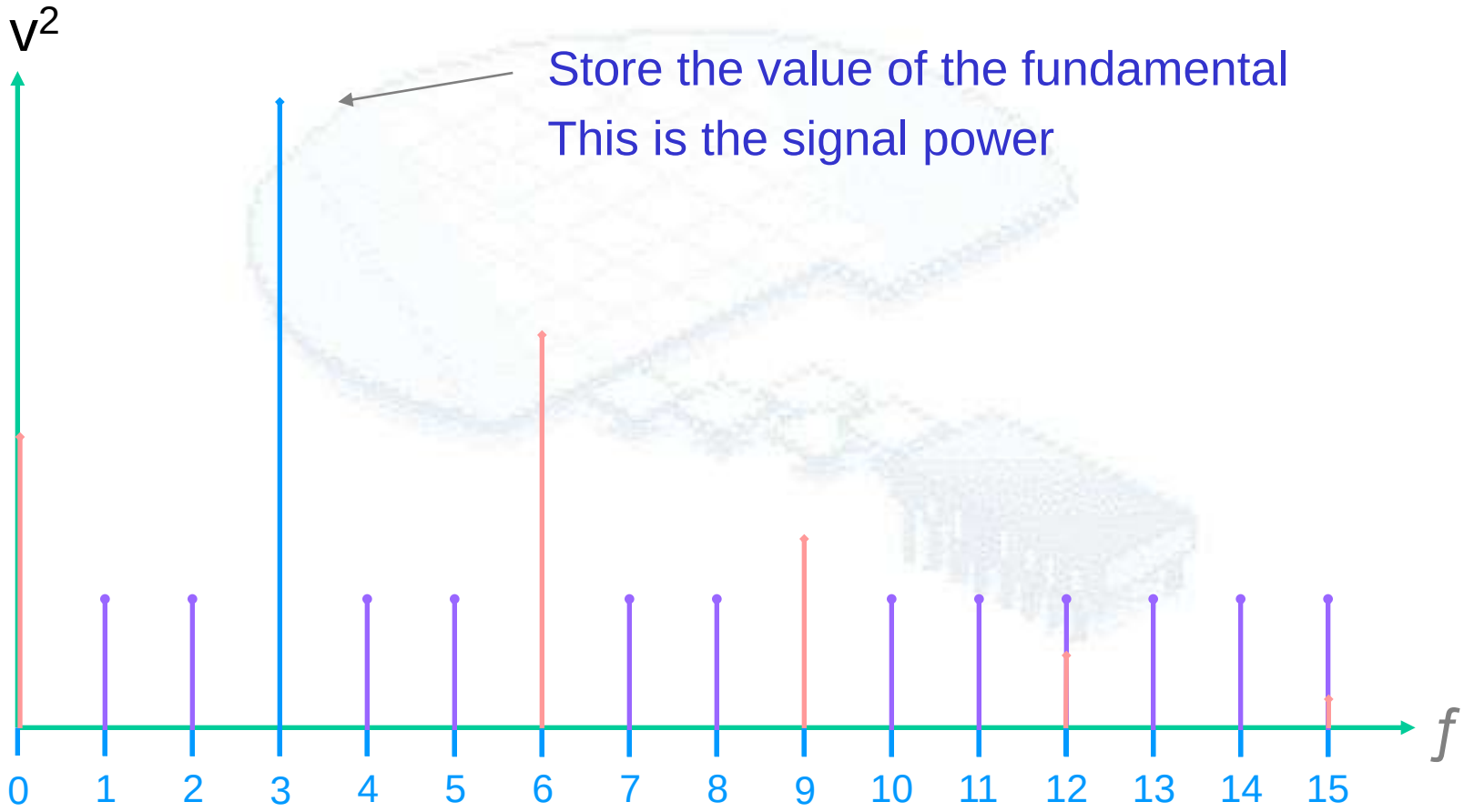
- This is the same methodology as computing SNR. However, now power of the harmonics is added to the noise power.
- Only zero out the DC component.

$$SNR = \frac{S}{N} \qquad THD = \frac{D}{S} \qquad SINAD = \frac{S}{N+D}$$

$$SNR^{-1} + THD = \frac{N}{S} + \frac{D}{S} = \frac{N+D}{S} = SINAD^{-1}$$

$$SINAD = (SNR^{-1} + THD)^{-1}$$

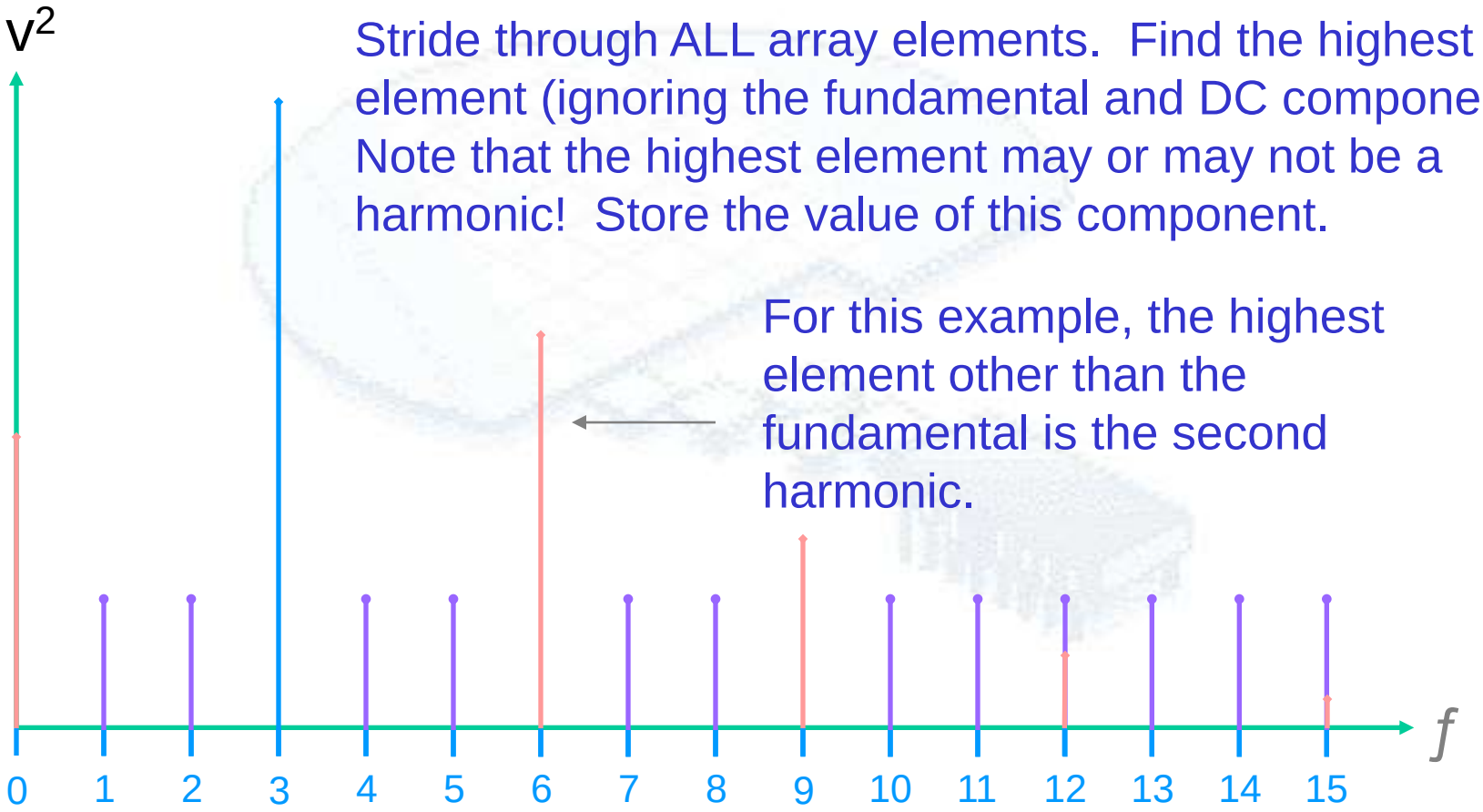
Spurious Free Dynamic Range (SFDR)



Power Spectrum

Revised 8/8/2007

Spurious Free Dynamic Range (SFDR)



Power Spectrum

Revised 8/8/2007

Spurious Free Dynamic Range (SFDR)

- Expressed in decibels (dB)
- The spurious free dynamic range is a positive value (assuming the fundamental is greater than the next highest spur power)

$$SFDR_{dB} = 10 \log_{10} \left[\frac{\text{Fundamental}}{\text{Next Highest}} \right]$$

Generic Mixed Signal Tester Architecture

PATTERN DATA SEQUENCER

SOURCE MEM

PATTERN MEM

CAPTURE MEM

WAVEFORM DATA TO TESTER CPU / DSP PROC

WAVEFORM DATA FROM TESTER CPU

USER CPU

TIMING AND FORMATTING

CLOCKS + SYNC

TESTER CPU + DSP PROC

DIGITAL HSD

DUT

TIME MEAS SUB-SYSTEM

DC METER

V/I SOURCES

RELAY MATRIX AND OTHER CONNECTION PATHS TO DUT

VOLTMETER

AC SRC

AC DIG

TERADYNE

Arbitrary Waveform Generator

PATTERN DATA SEQUENCER

WAVEFORM DATA FROM TESTER CPU

SOURCE MEM

PATTERN MEM

CAPTURE MEM

WAVEFORM DATA TO TESTER CPU / DSP PROC

USER CPU

TIMING AND FORMATTING

CLOCKS + SYNC

TESTER CPU + DSP PROC

DRIVE AND COMPARATOR CHANNELS

DUT

TIME MEAS SUB-SYSTEM

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RELAY MATRIX AND OTHER CONNECTION PATHS TO DUT

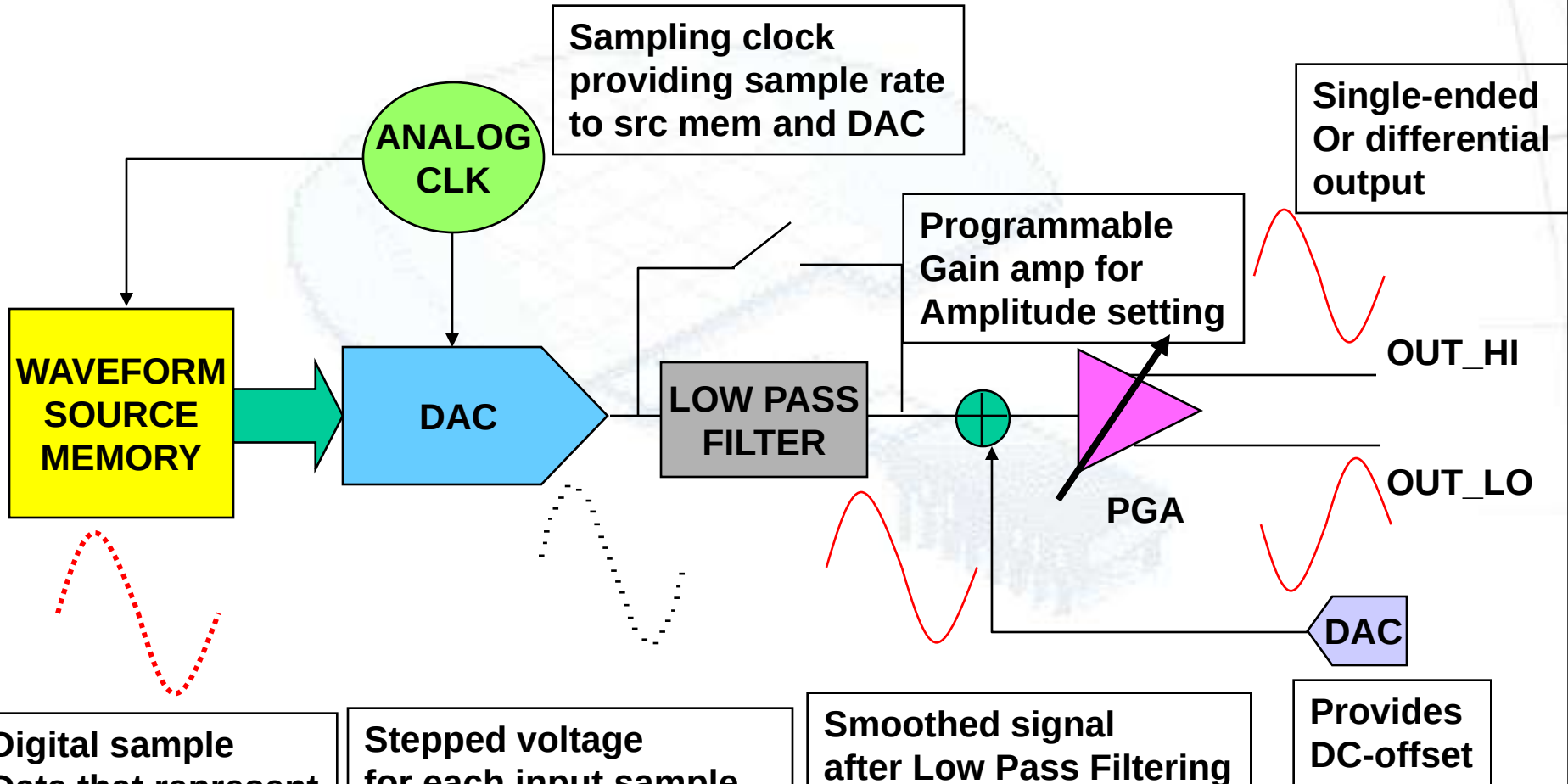
VOLTMETER

AC SRC

AC DIG

TERADYNE

ARBITRARY WAVEFORM GENERATOR



IMPORTANT PARAMETERS OF AN AWG

- Maximum Peak to Peak Voltage output
- Waveform resolution (DAC resolution)
- Band-width
- Waveform source memory depth
- Output Impedance
- Noise, THD, SNR

PATTERN DATA SEQUENCER

WAVEFORM DATA FROM TESTER CPU

SOURCE MEM

PATTERN MEM

CAPTURE MEM

WAVEFORM DATA TO TESTER CPU / DSP PROC

USER CPU

TIMING AND FORMATTING

CLOCKS + SYNC

TESTER CPU + DSP PROC

DRIVE AND COMPARATOR CHANNELS

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RELAY MATRIX AND OTHER CONNECTION PATHS TO DUT

VOLTMETER

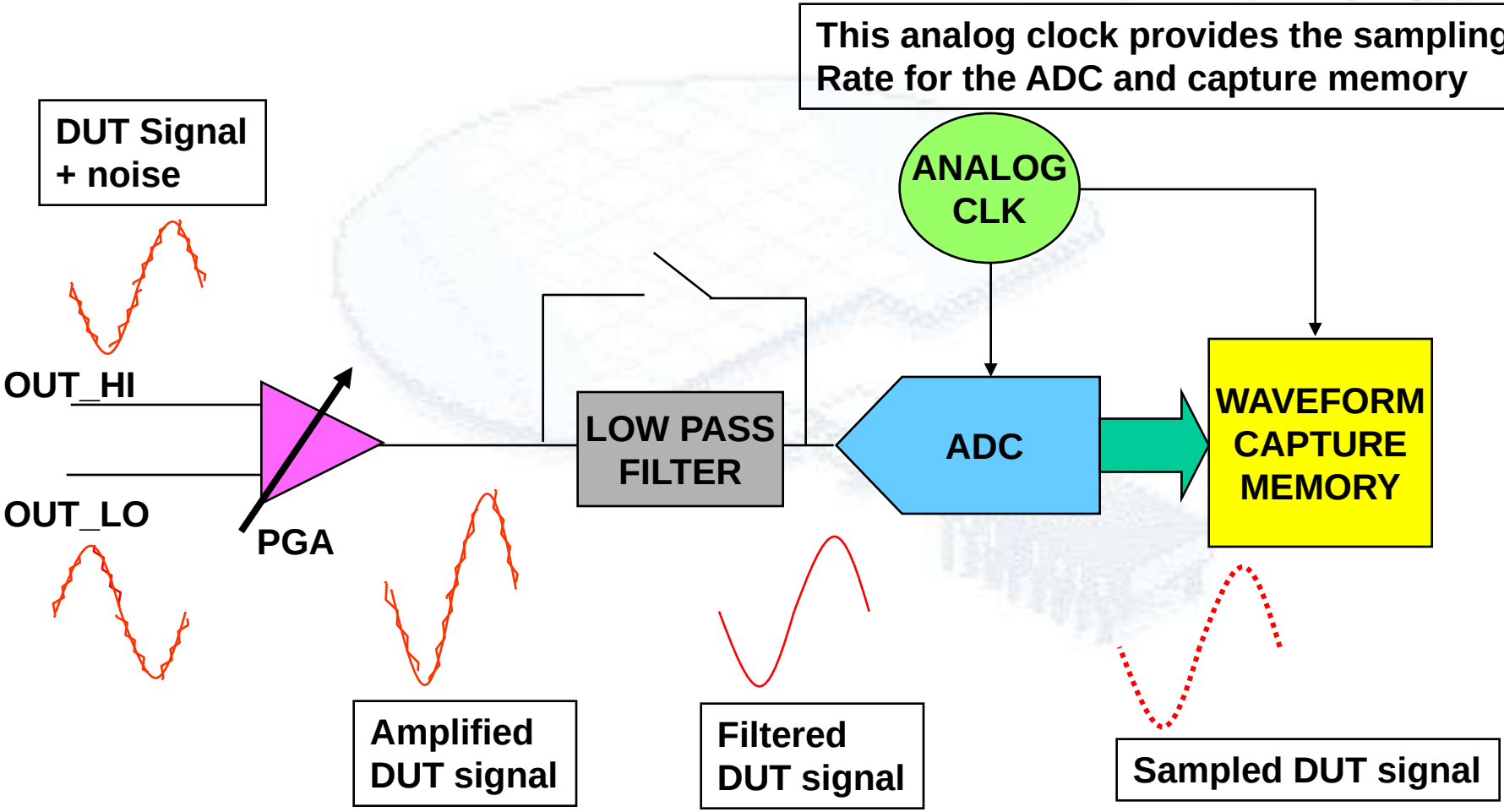
AC SRC

AC DIG

Waveform Digitizer

TERADYNE

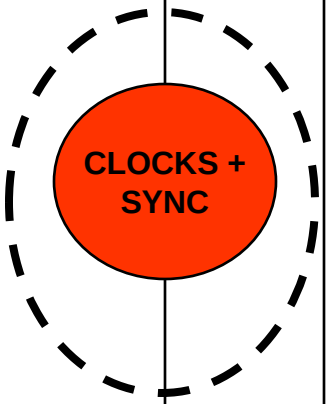
WAVEFORM DIGITIZER



IMPORTANT PARAMETERS OF A WAVEFORM DIGITIZER

- Maximum Peak to Peak input Voltage range
- Waveform resolution (ADC resolution)
- Band-width
- Waveform capture memory depth
- Input Impedance
- Noise, THD, SNR, spur

Digital-Analog Synchronization



ac src trigger from sequencer

PATTERN DATA SEQUENCER

SOURCE MEM

PATTERN MEM

CAPTURE MEM

TIMING AND FORMATTING

USER CPU

TESTER CPU + DSP PROC

DUT

DC METER

TIME MEAS SUB-SYSTEM

V/I SOURCES

RELAY MATRIX AND OTHER CONNECTION PATHS TO DUT

VOLTMETER

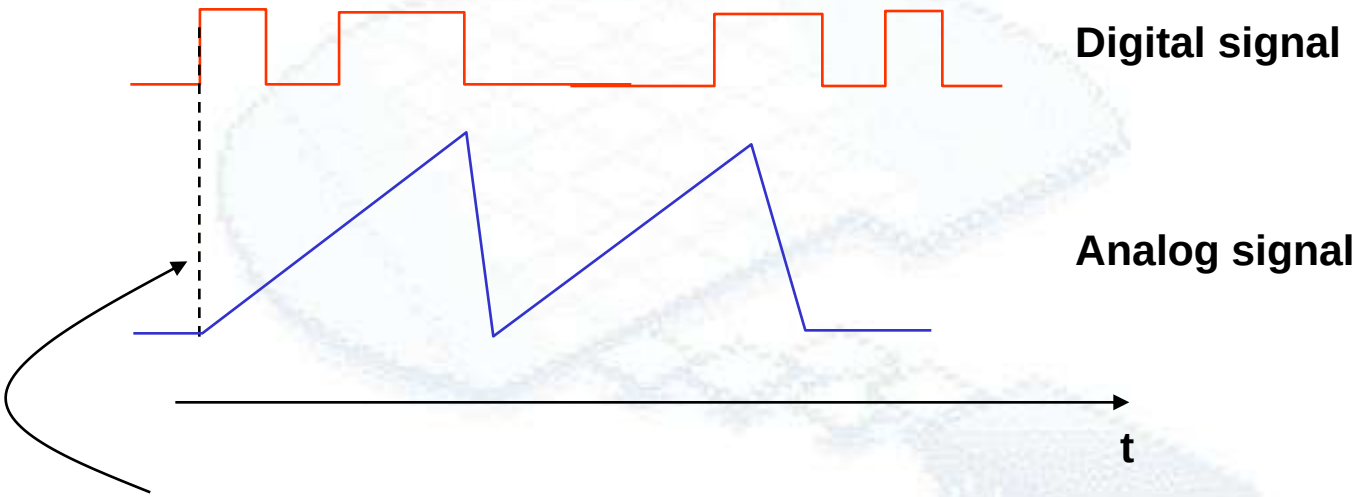
AC SRC

AC DIG

Ac dig trigger from sequencer

TERADYNE

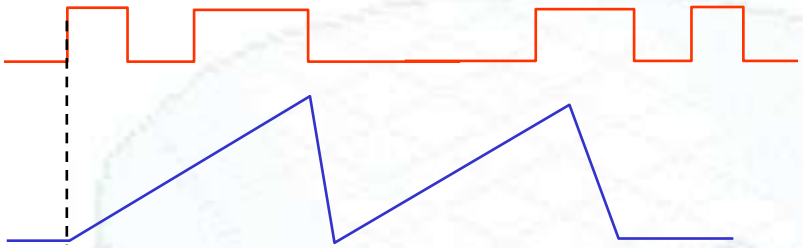
WHY SYNCHRONIZATION?



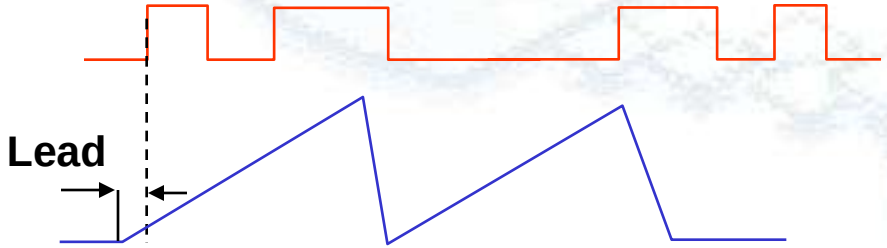
If this alignment is crucial for DUT operations, the digital sub-system must have the capability to send a trigger to the analog sub-system source at a precise t0 cycle.

REPEATABILITY

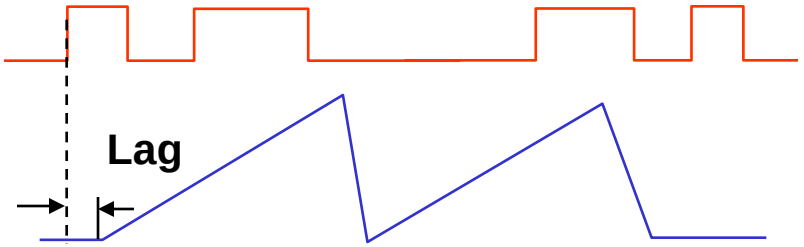
1.



2.



3.

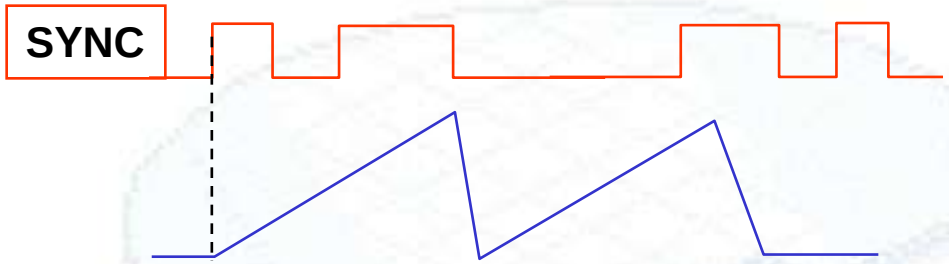


The analog clock that provides the sample rate to the AC src is seen to not have a fixed phase relationship to t0.Rather, it will have a random phase shift with respect to t0. This causes the run to run Sync error by one analog clock cycle which can be multiples of t0.

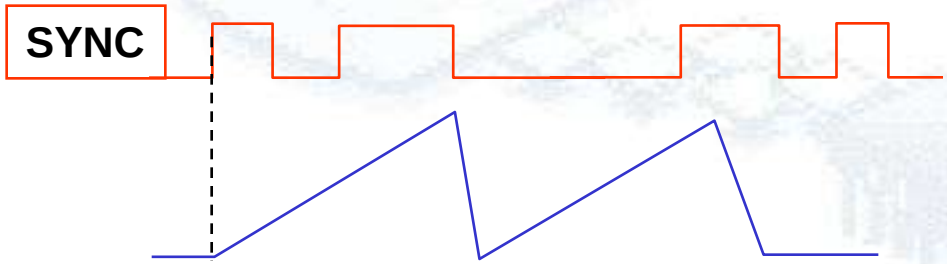
Revised 8/8/2007

REPEATABILITY

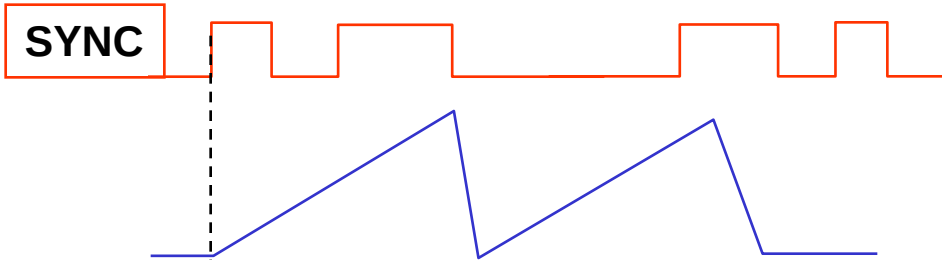
1.



2.



3.



To ensure that the analog clock and the t0 is at a known phase relation-ship at every run, a syncing routine between the t0 and analog clock must be done prior to starting the signals. This syncing routine actually aligns the clocks together.

PATTERN DATA SEQUENCER

SOURCE MEM

PATTERN MEM

CAPTURE MEM

Waveform Data To Tester CPU / DSP Proc

USER CPU

TIMING AND FORMATTING

CLOCKS + SYNC

TESTER CPU + DSP PROC

Digital Signal Processing

DUT

TIME MEAS SUB-SYSTEM

DC METER

V/I SOURCES

RELAY MATRIX AND OTHER CONNECTION PATHS TO DUT

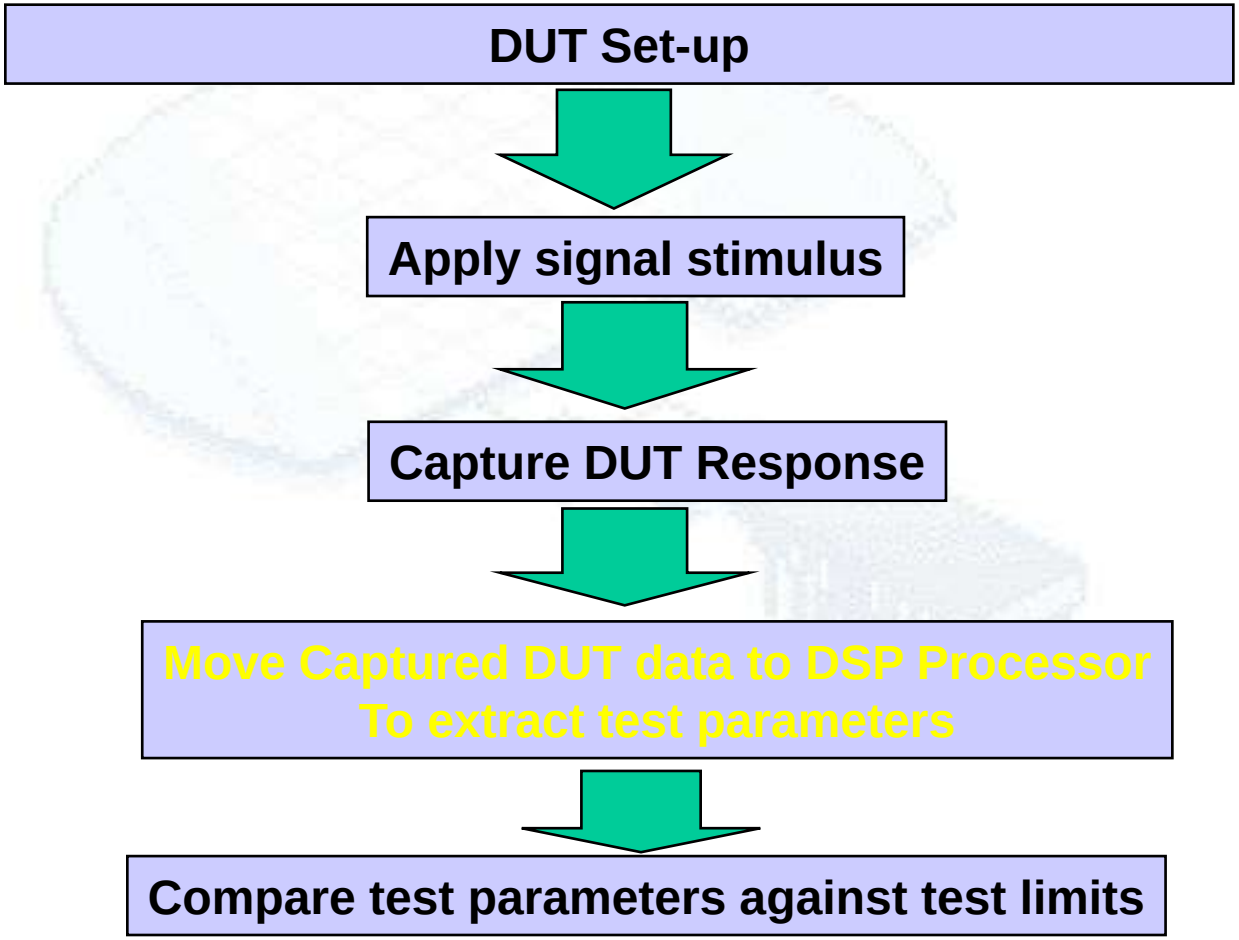
AC SRC

AC DIG

Captured analog Waveform data Moved to DSP proc

Revised 8/8/2007

Test Flow



Revised 8/8/2007

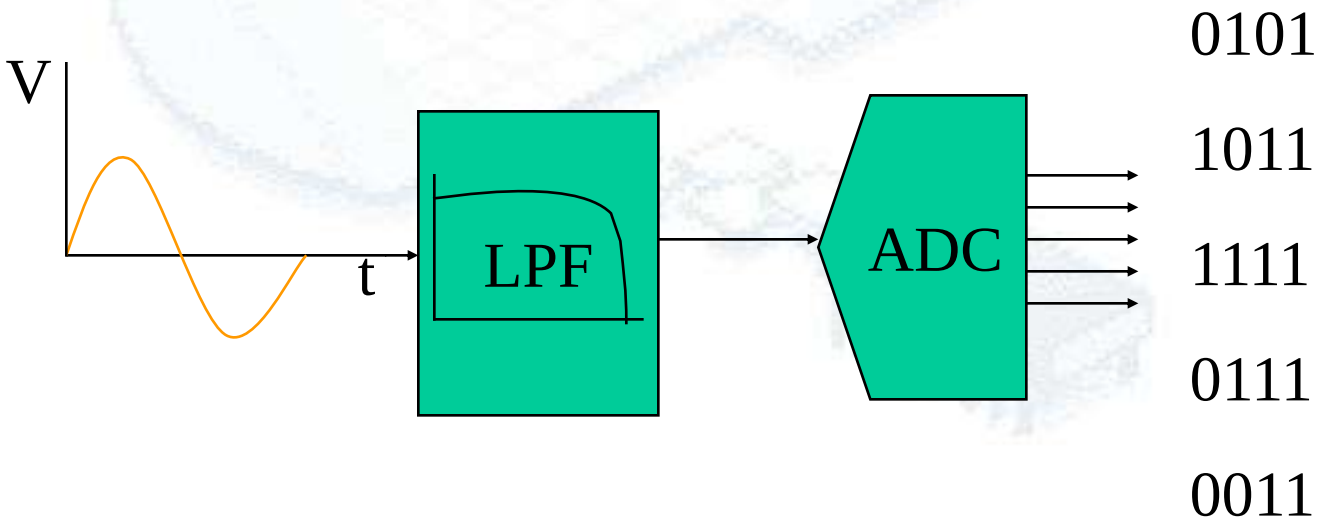
Self-Assess Questions

- What is the definition of a mixed signal circuit?
- What is the difference between FFT and DFT algorithm?
- How can leakage be avoided that may be caused by the test system?
- What is coherent sampling?
- If 128 samples are taken at 50usec intervals from 7 complete cycles,
  - What is the UTP?
  - What is the Fres?
  - What is the signal frequency?

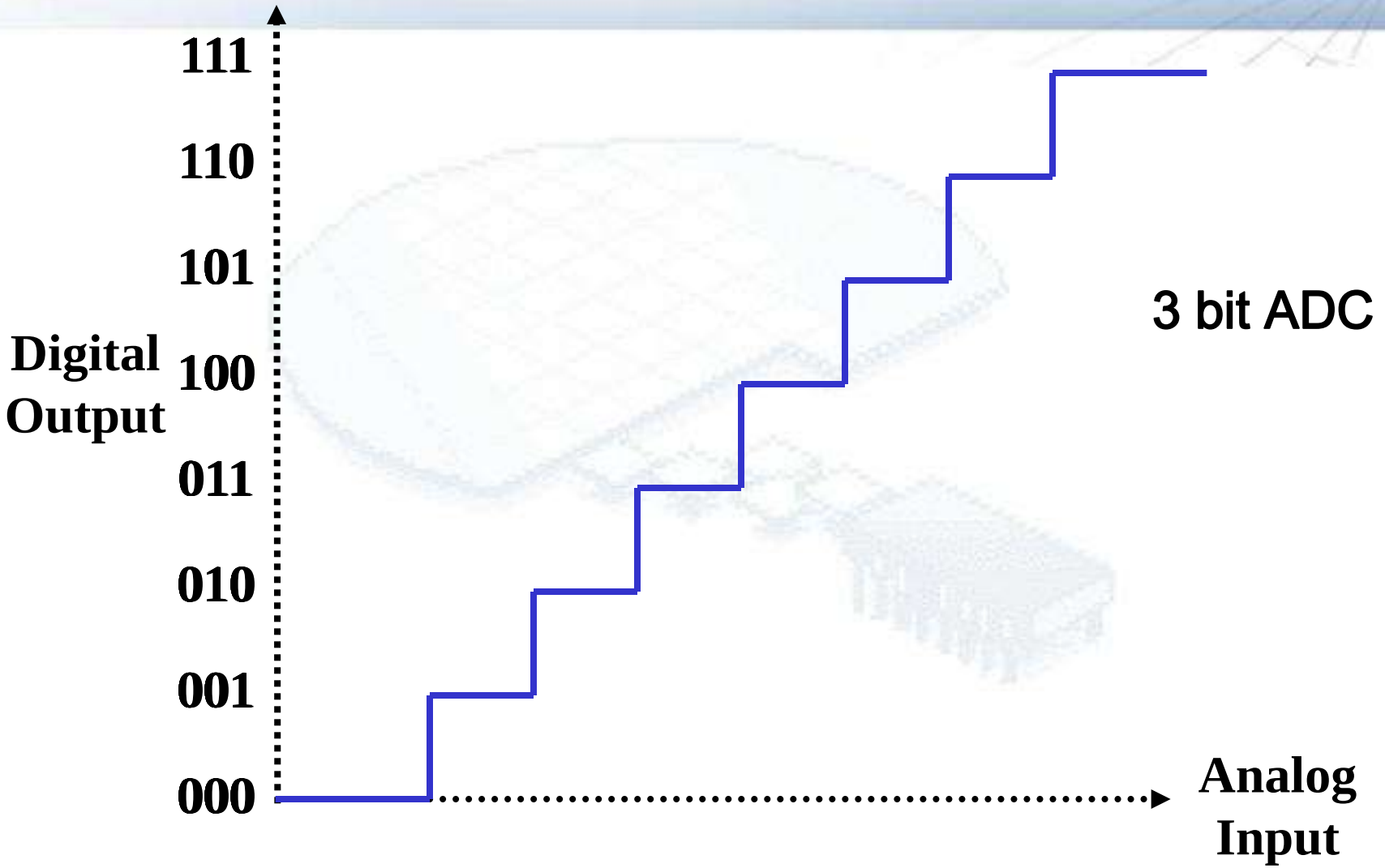
ADC TESTING

Analog-to-Digital Converter

An ADC is used to convert analog signals to digital data



Analog-to-Digital Converter



ADC STATIC PARAMETERS

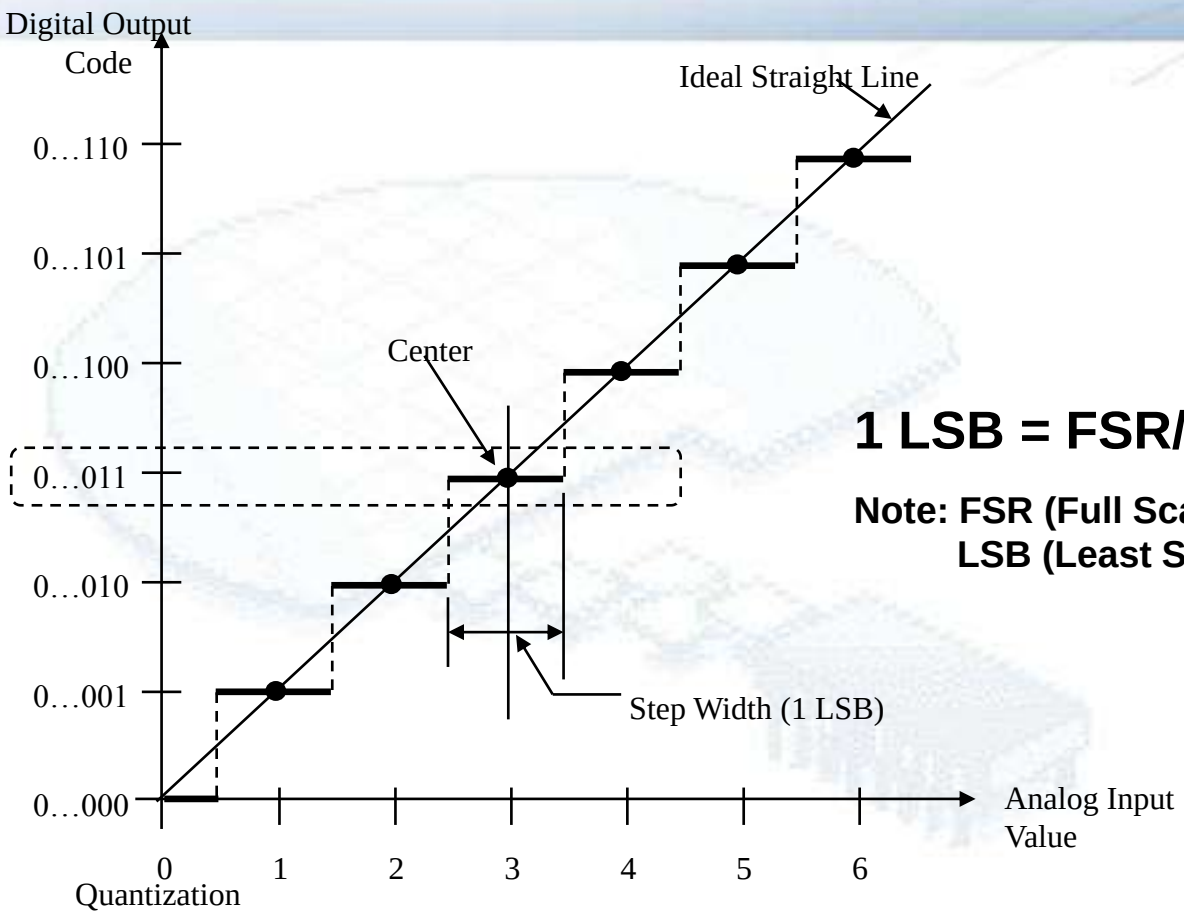
The ideal transfer function for an ADC is a straight line but the actual ideal result is a uniform staircase where the number of steps corresponds to the number of digital output codes. Since analog is continuous and digital is discrete this results in quantization process which introduces an error (quantization error).

The width of one step is 1 LSB (least significant bit). The resolution of an ADC is normally expressed as number of bits (digital output code). An ADC with an n-bit resolution has 2^n possible digital codes which define 2^n step levels. But the first (zero) step and the last (all ones) are only one half of a full width thus the full-scale range (FSR) is divided into 2^n –1 step widths. Thus one LSB is:

$$1\ LSB = FSR /(2^n-1)\ \text{for an n-bit converter}$$

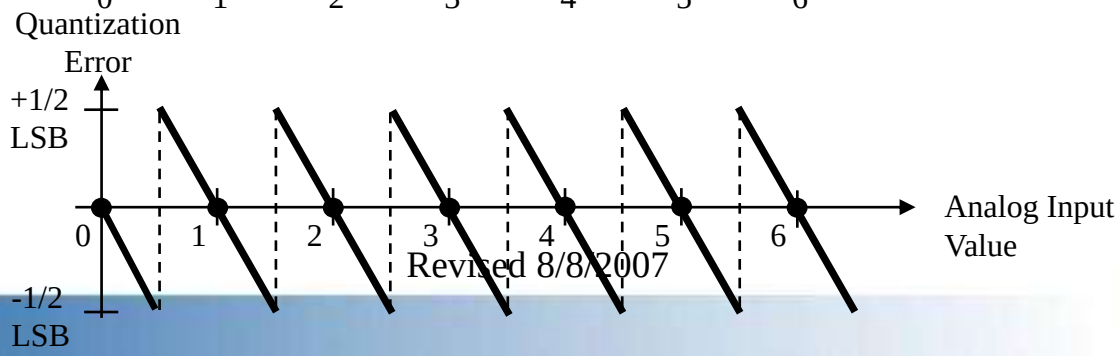
ADC STATIC PARAMETERS

Analog Input Values	Digital Output Code
5.5-6.5	0…110
4.5-5.5	0…101
3.5-4.5	0…100
2.5-3.5	0…011
1.5-2.5	0…010
0.5-1.5	0…001
0.0-0.5	0…000

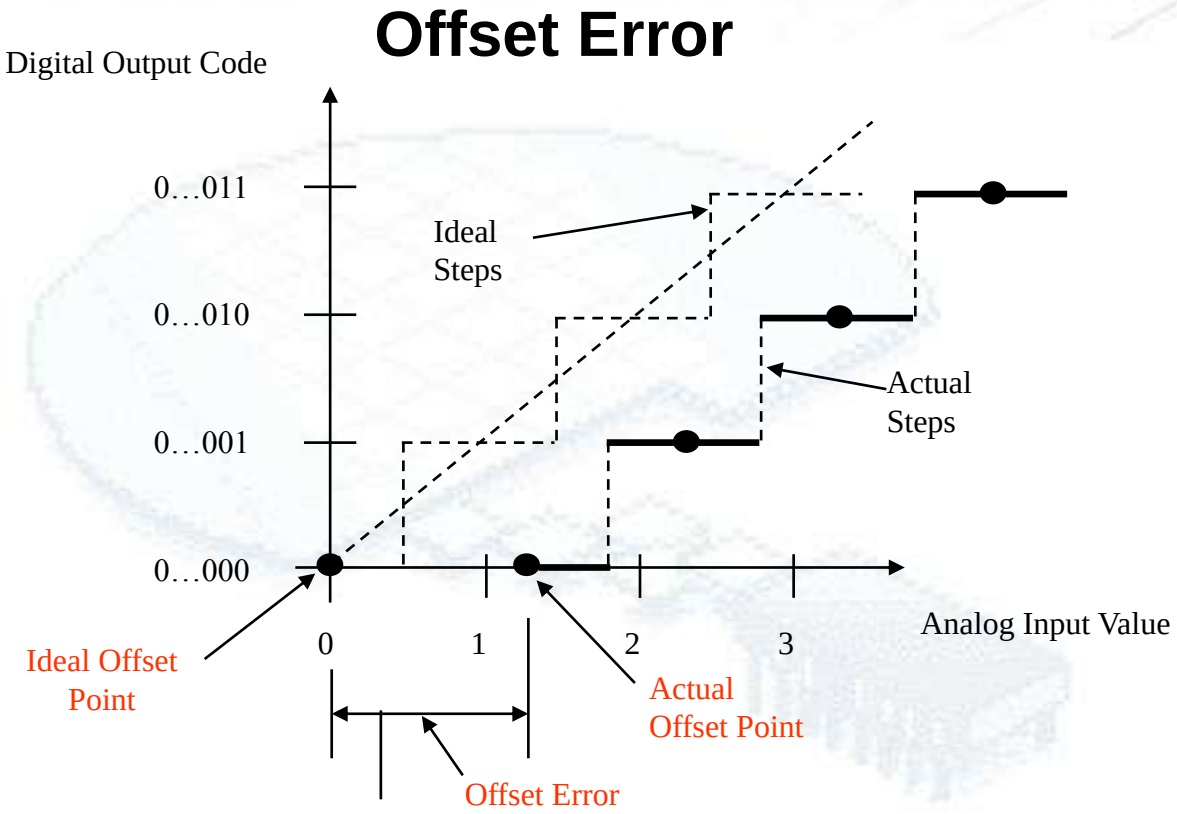


1 LSB = FSR/ (2^n – 1)

Note: FSR (Full Scale Range)
LSB (Least Significant Bit)



ADC STATIC PARAMETERS

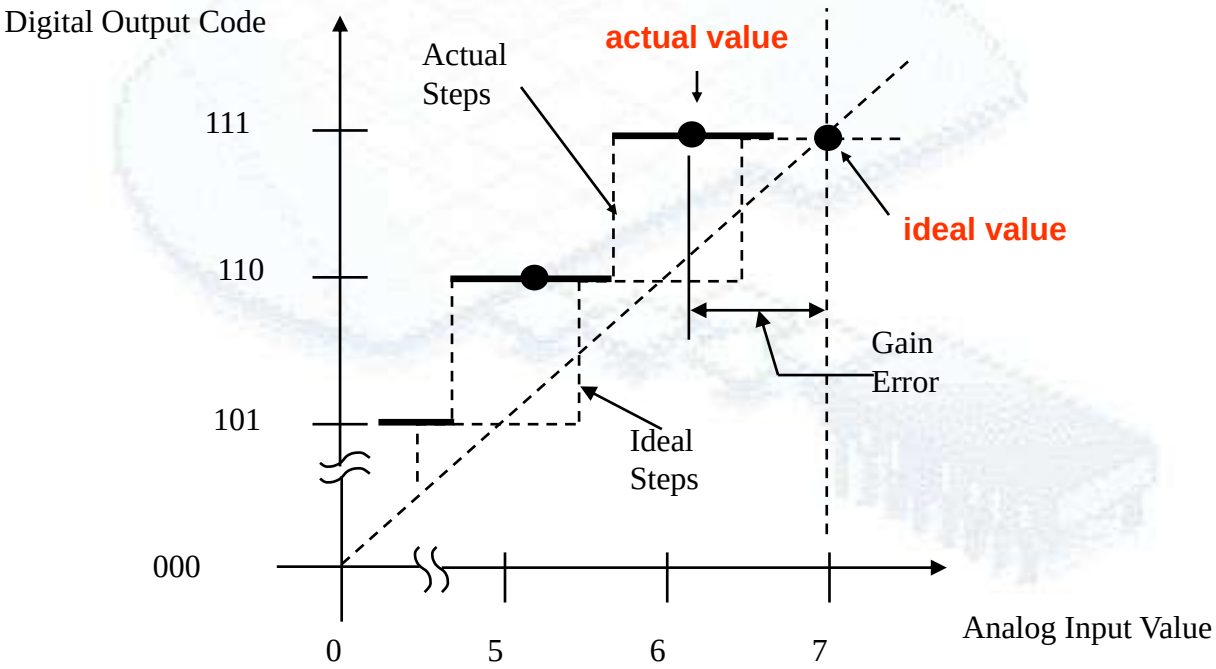


Offset Error (also called zero-scale error) is the difference between ideal and actual offset (initial) points. For the ADC the offset error is measured from the **midpoint of the zero step (ideal to actual).**

Revised 8/8/2007

ADC STATIC PARAMETERS

For ADC the gain point is the middle of the full scale output step.



Gain Error is the difference between ideal and actual gain points on the transfer function after the offset error has been corrected to zero.

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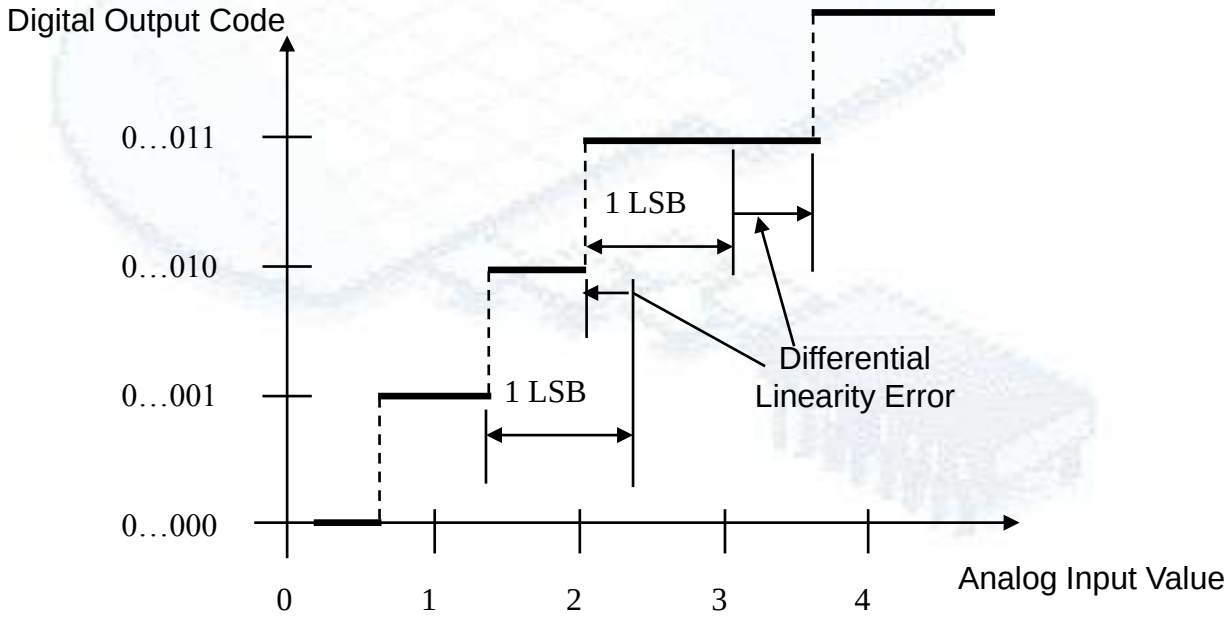
ADC STATIC PARAMETERS

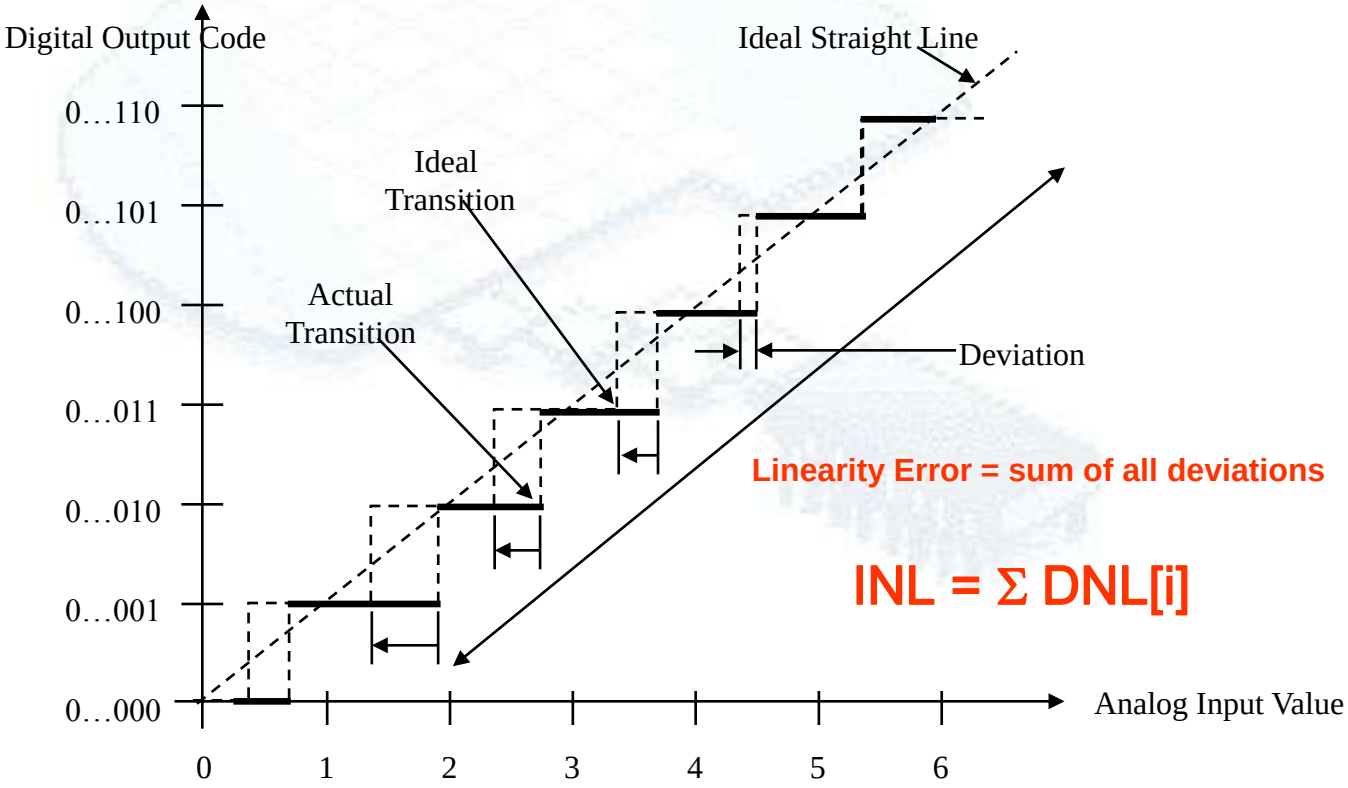
DNL Error is the difference between an actual step width and an ideal step width (1 LSB). If DNL Error is too large, there can be missing codes, where one or more of the codes never receive an output.



Differential Non Linearity (DNL)

ADC STATIC PARAMETERS

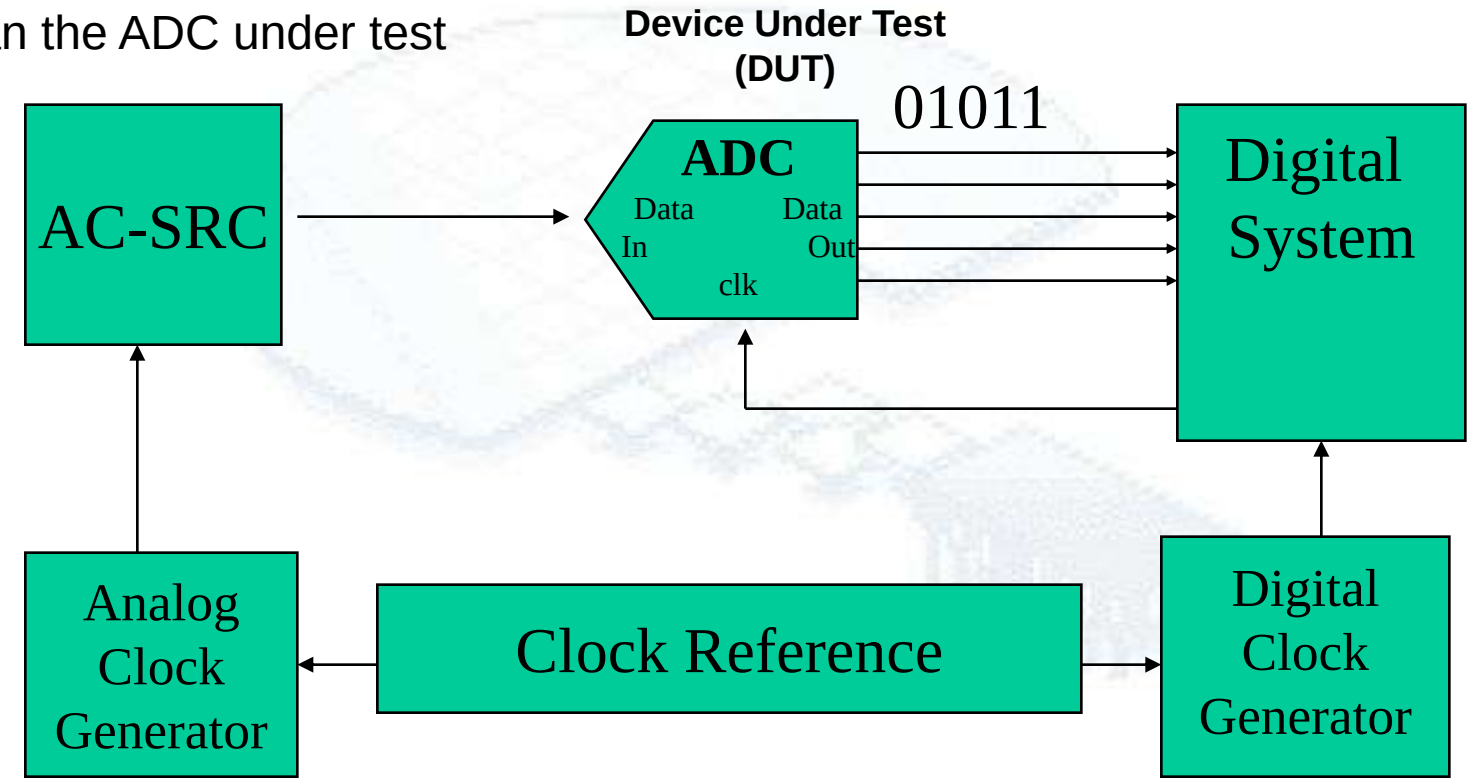
INL Error is the deviation of the values of the actual step function to the ideal straight line function. For ADC, the deviations are measured at the transition points from one step to the next.



Integral Non Linearity (INL)

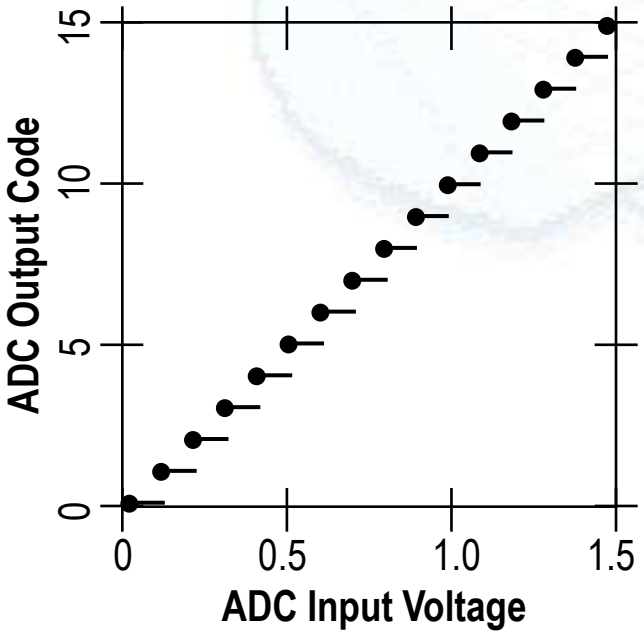
ADC TEST SETUP

AC Source should be
2-4 bits more resolution
than the ADC under test



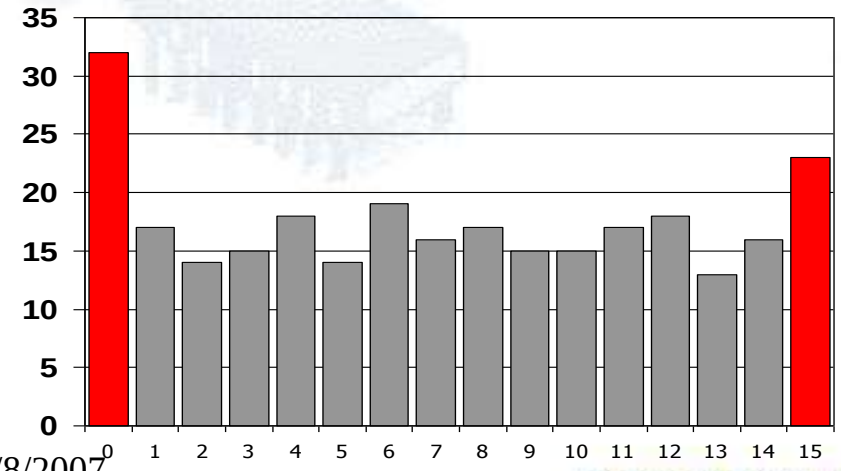
ADC STATIC TEST METHODOLOGY

The ADC voltage-to-code transfer curve is a many-to-one mapping function.

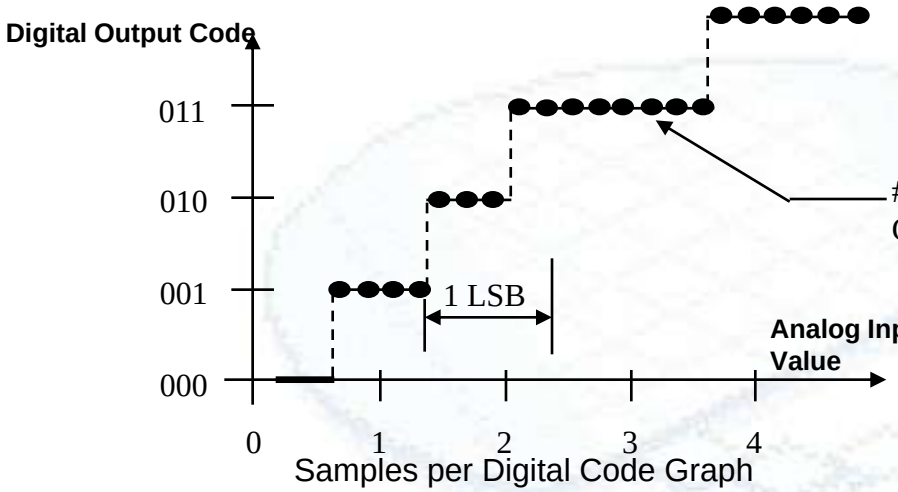


Fundamental measurement : measure the voltage corresponding to the transition from one digital code to the next (decision level, code edge).

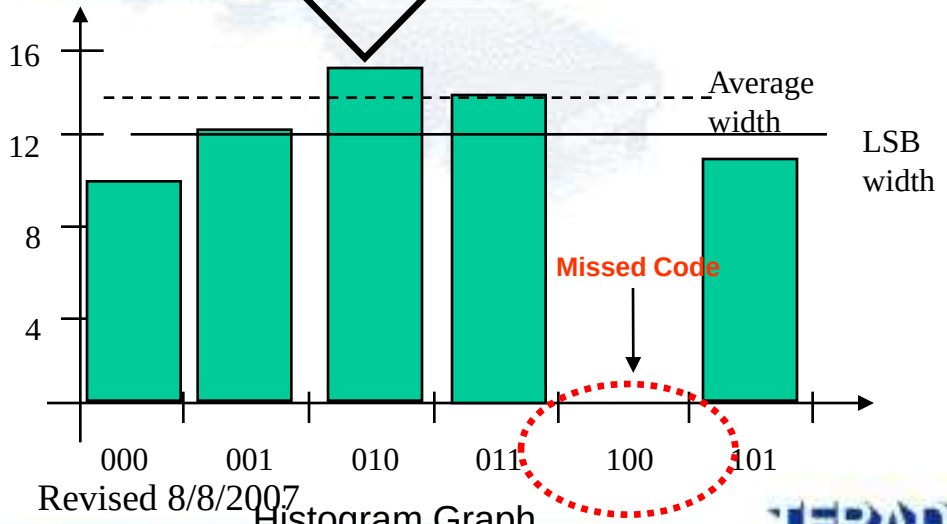
Practical test technique: linear ramp histogram method (**code width measurement**). The input ramp is slow enough to give a statistically relevant "number of hits per code".



ADC STATIC TEST METHODOLOGY



Samples per Digital Code Graph



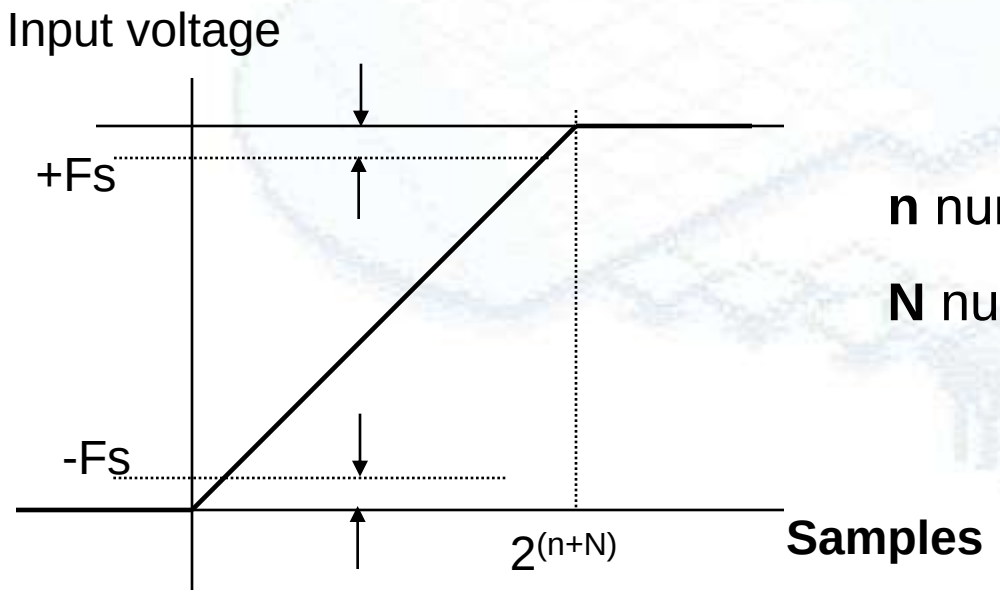
Histogram Graph

Revised 8/8/2007

ADC STATIC TEST METHODOLOGY

Histogram Method

Make a ramp wave segment for ACSRC. The input ramps goes above and below +Fs/-Fs to assure that all codes are covered.



n number of ADC's bits

N number of additional bits (=4)

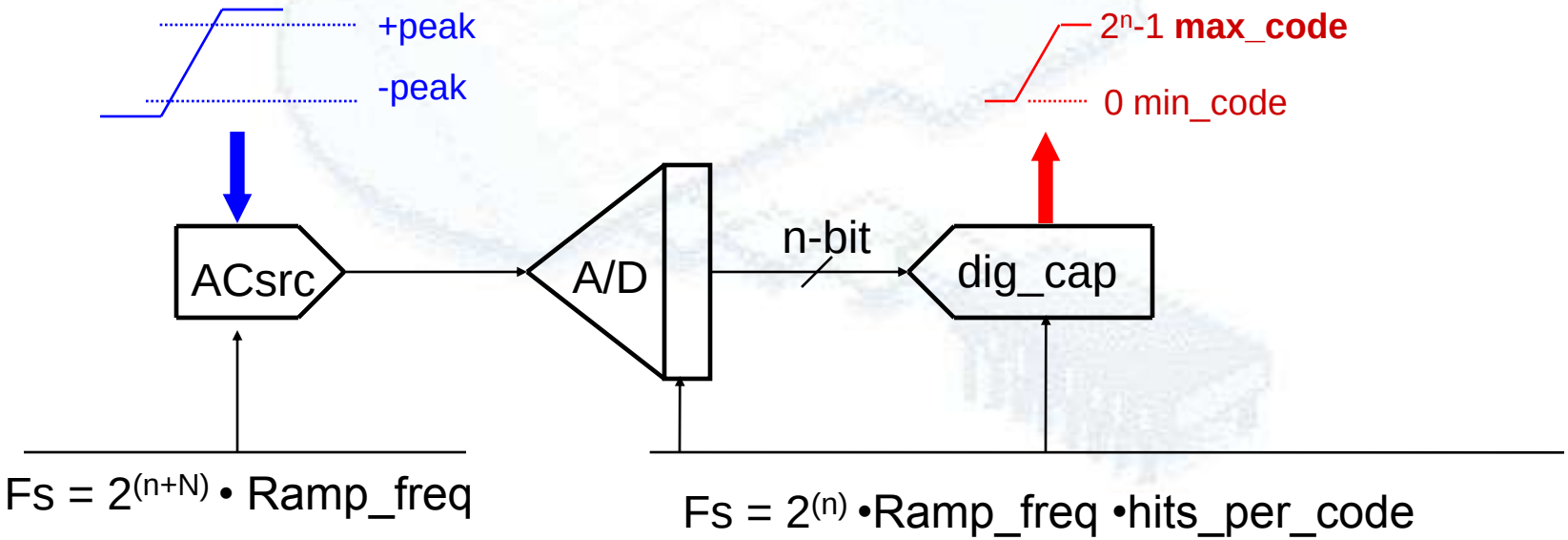
Resolution of ac source ≥ 1/16 (resolution of ADC)

Linearity of ac source = 1/16 (resolution of ADC)

ADC STATIC TEST METHODOLOGY

Histogram Method

Block diagram of signal setup

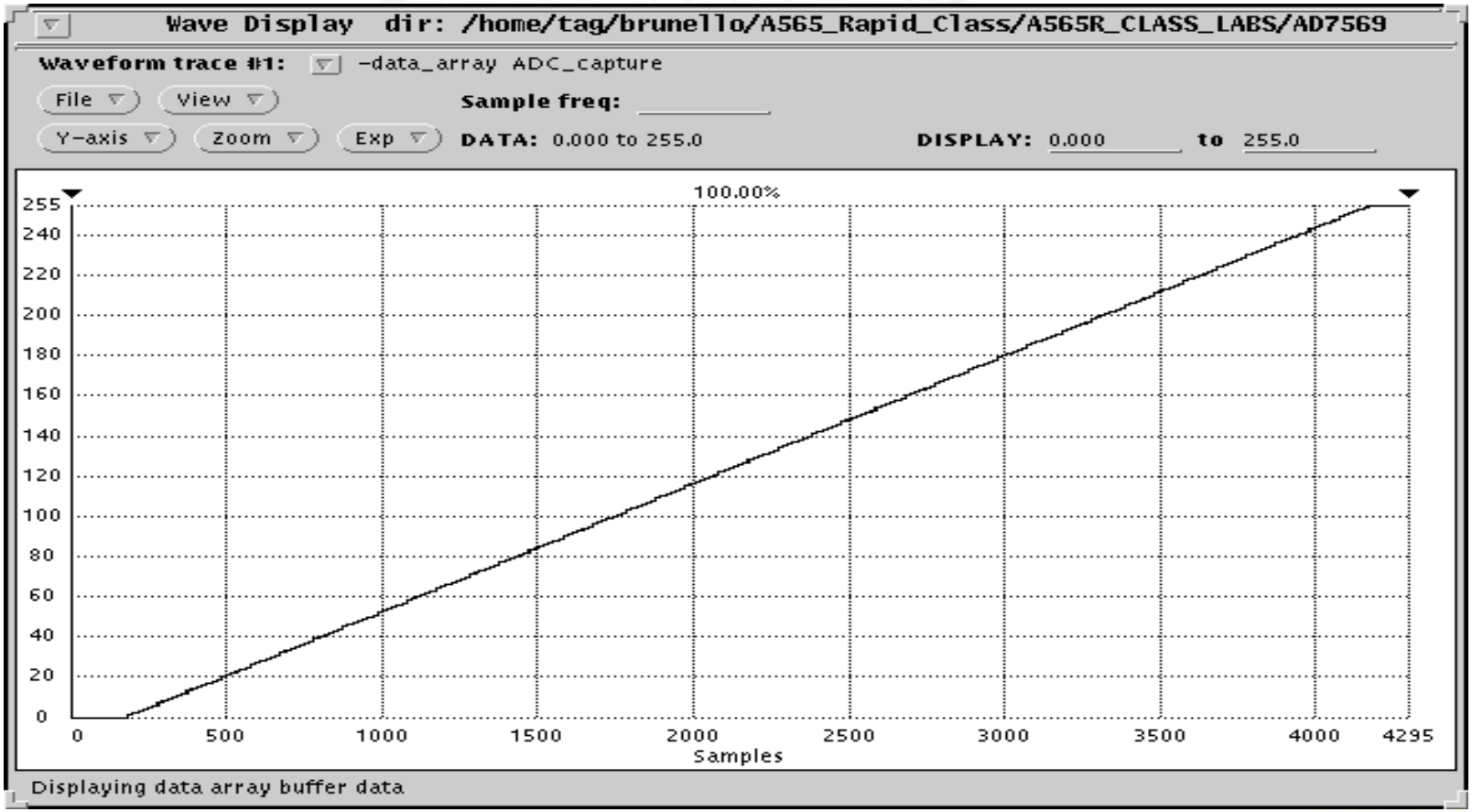


Samples_captured = $2^{(n)}$. hits_per_code

ADC STATIC TEST METHODOLOGY

Histogram Method

Capture the Ramp wave

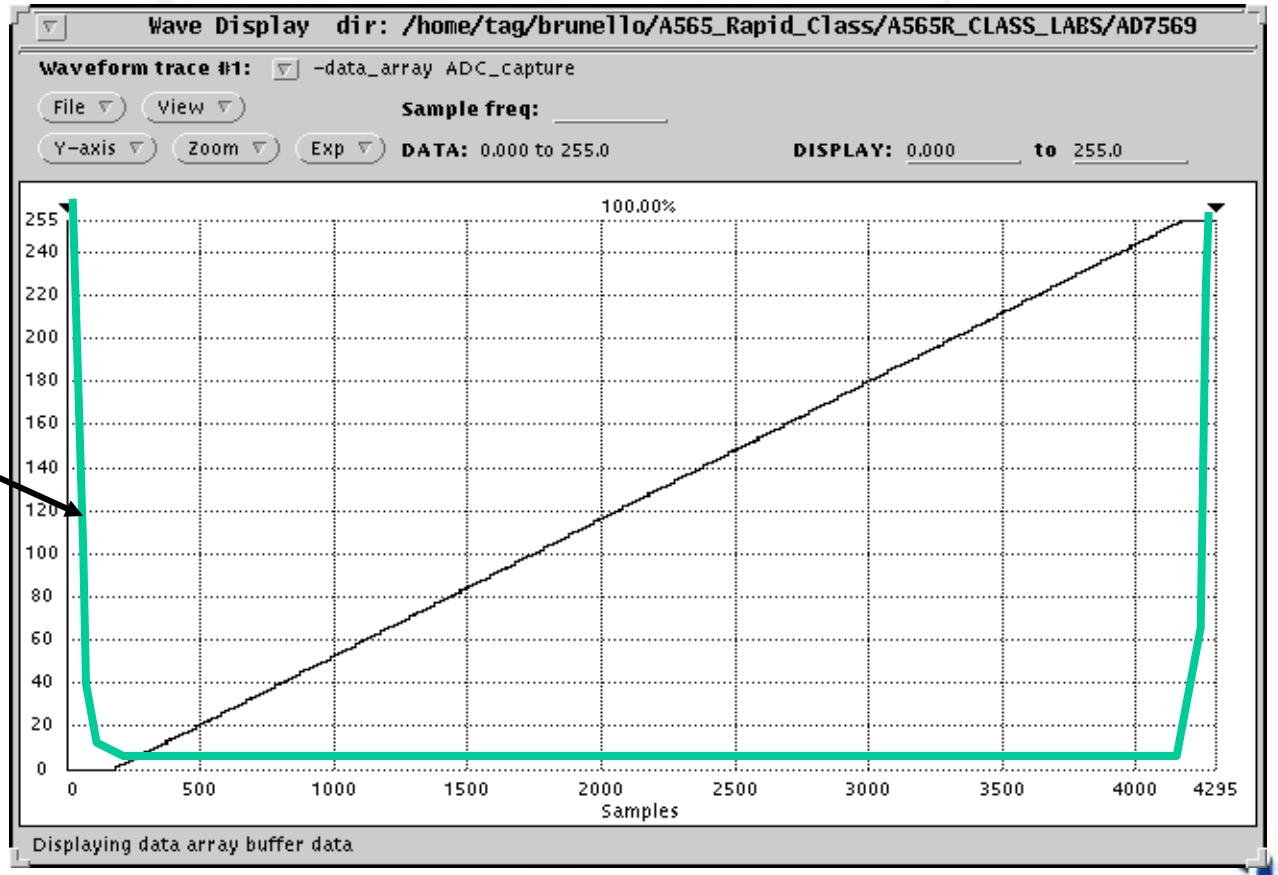


ADC STATIC TEST METHODOLOGY

Histogram Method

Use DSP algorithm to generate a histogram plot of the captured ramp

Histo-plot

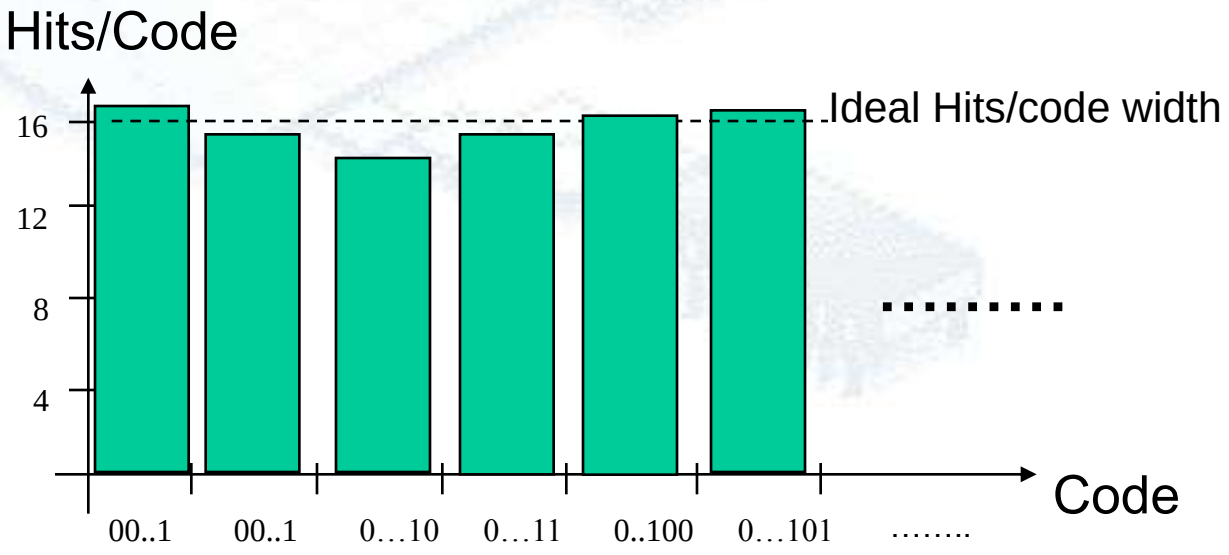


ADC STATIC TEST METHODOLOGY

Histogram Method

Take data between the start of ramp (min+1 code [0…01]), to the end of the ramp (max-1 code [1…10]).

This gives you 2^n – 2 codes' worth of data.



Histogram Graph

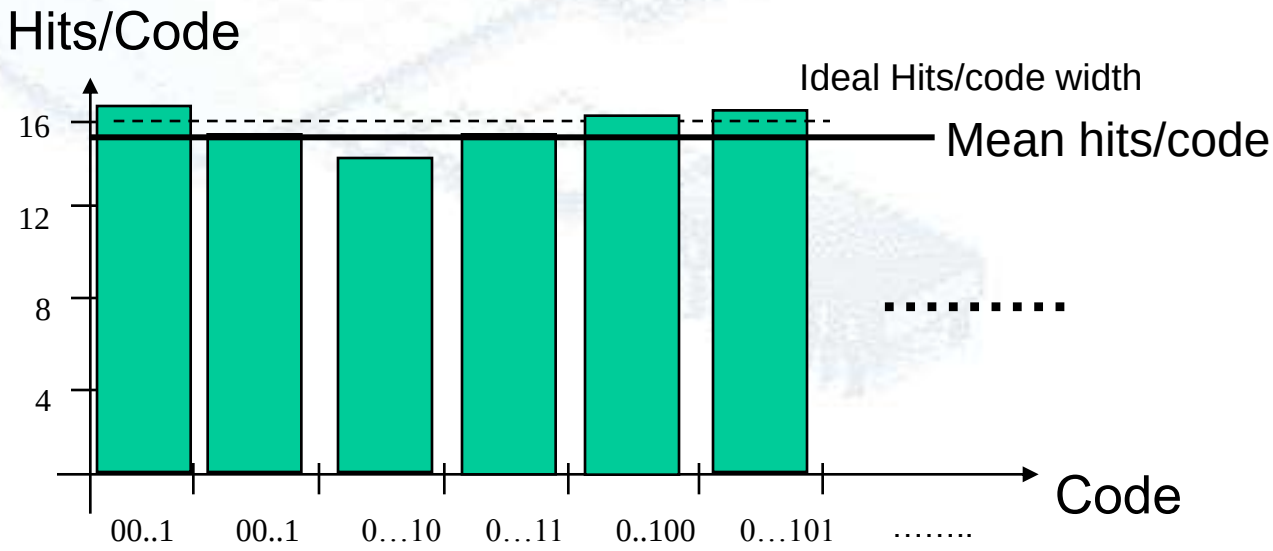
Revised 8/8/2007

ADC STATIC TEST METHODOLOGY

Histogram Method

$$\text{Calculate for DNL}[i] = \text{Hits}[i] - \frac{\sum \text{Hits}[i]}{2^n - 2}$$

$$\frac{\sum \text{Hits}[i]}{2^n - 2}$$



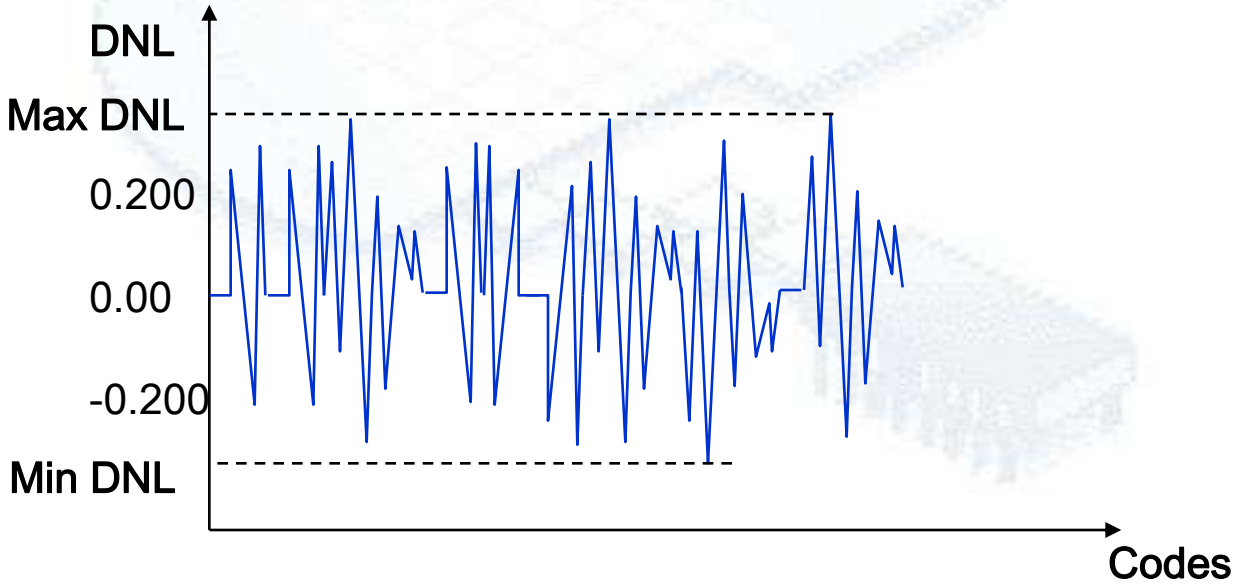
Histogram Graph

Revised 8/8/2007

ADC STATIC TEST METHODOLOGY

Histogram Method

Find max DNL and min DNL values:

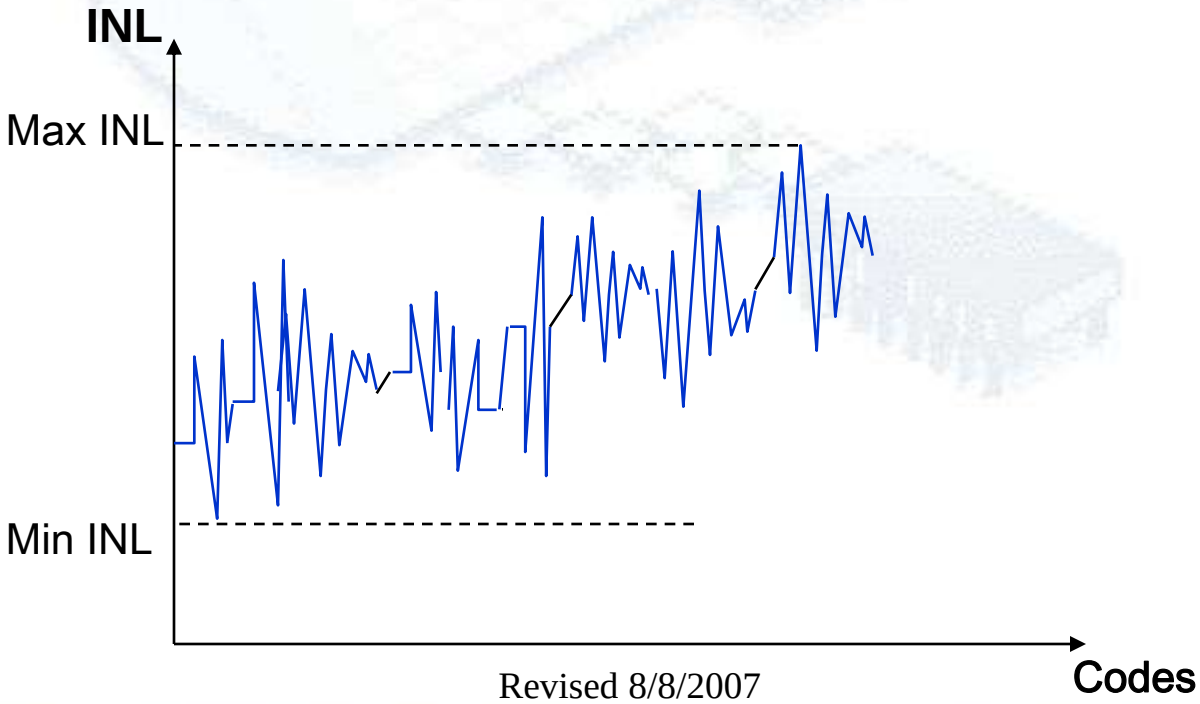


ADC STATIC TEST METHODOLOGY

Histogram Method

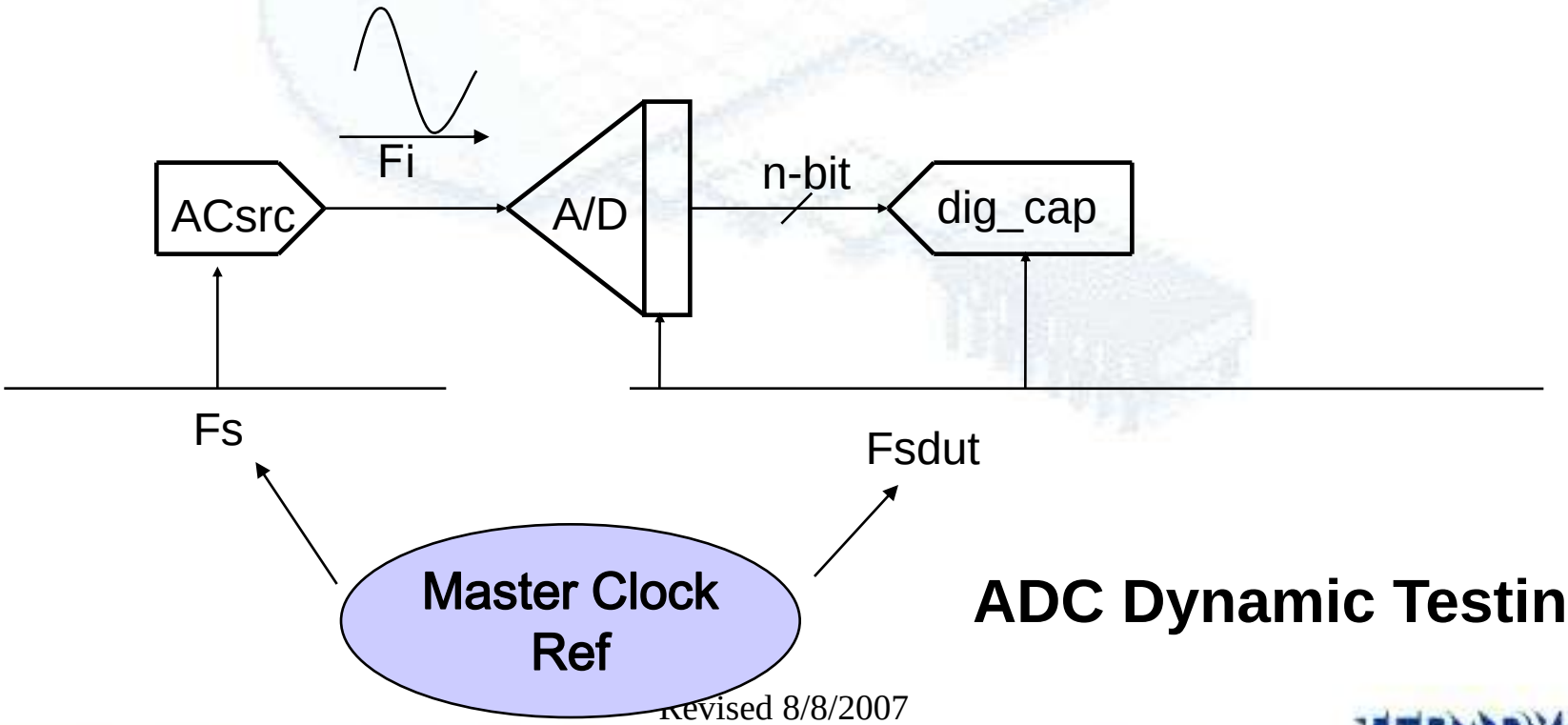
Calculate INL[i] = DNL[i]+DNL[i-1]+…..+DNL[0] for every i.

Get Max INL and Min INL



ADC DYNAMIC TEST METHODOLOGY

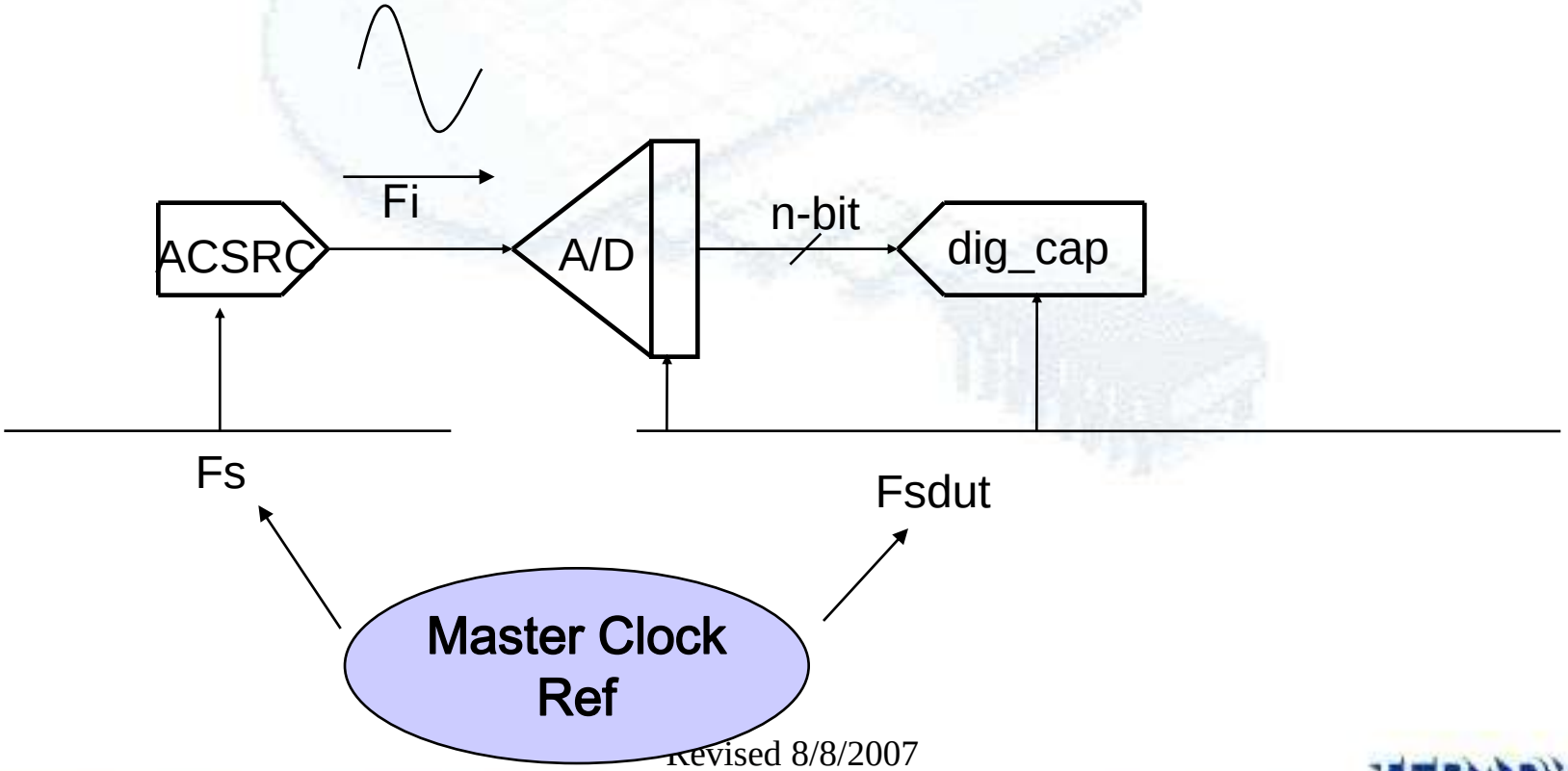
It is common practice to ensure the analog clock and the digital clock are referenced to a common master clock so that phase relation-ship of the clock sources are fixed and synchronized, making test results highly repeatable.



ADC Dynamic Testing

ADC DYNAMIC TEST METHODOLOGY

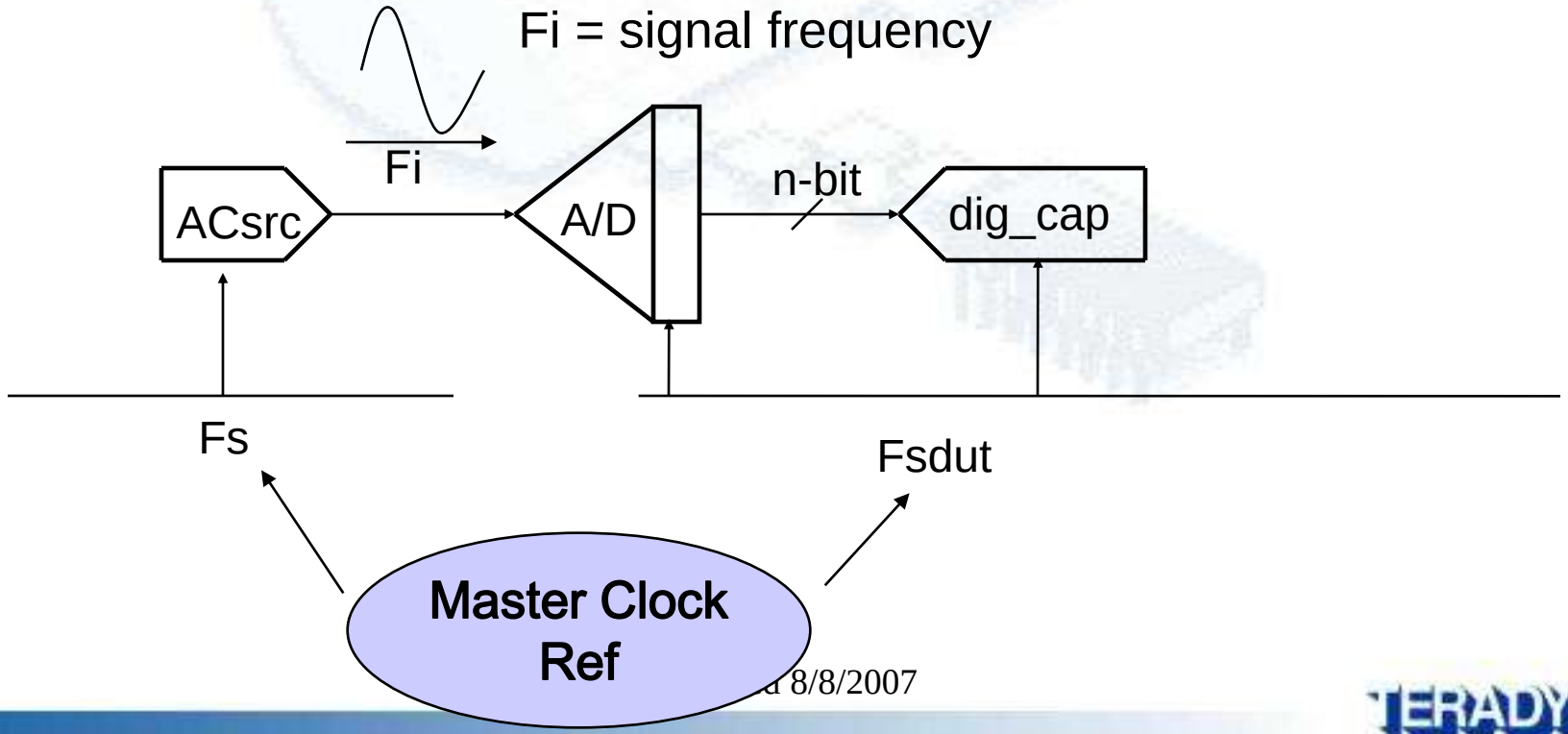
The ACSRC is used to supply a sinewave input to the ADC.
The output from the ADC (digital representation of the sinewave) is captured/sampled by the dig_cap.
Coherency of source and capture is important.



ADC DYNAMIC TEST METHODOLOGY

For digital capture:

Fsdut/Fi = Ncap/M
where,
Fsdut = ADC sampling rate= dig_cap sample rate
Ncap = # of samples captured (2^x number)
Mc = # of integer cycles (odd)
Fi = signal frequency

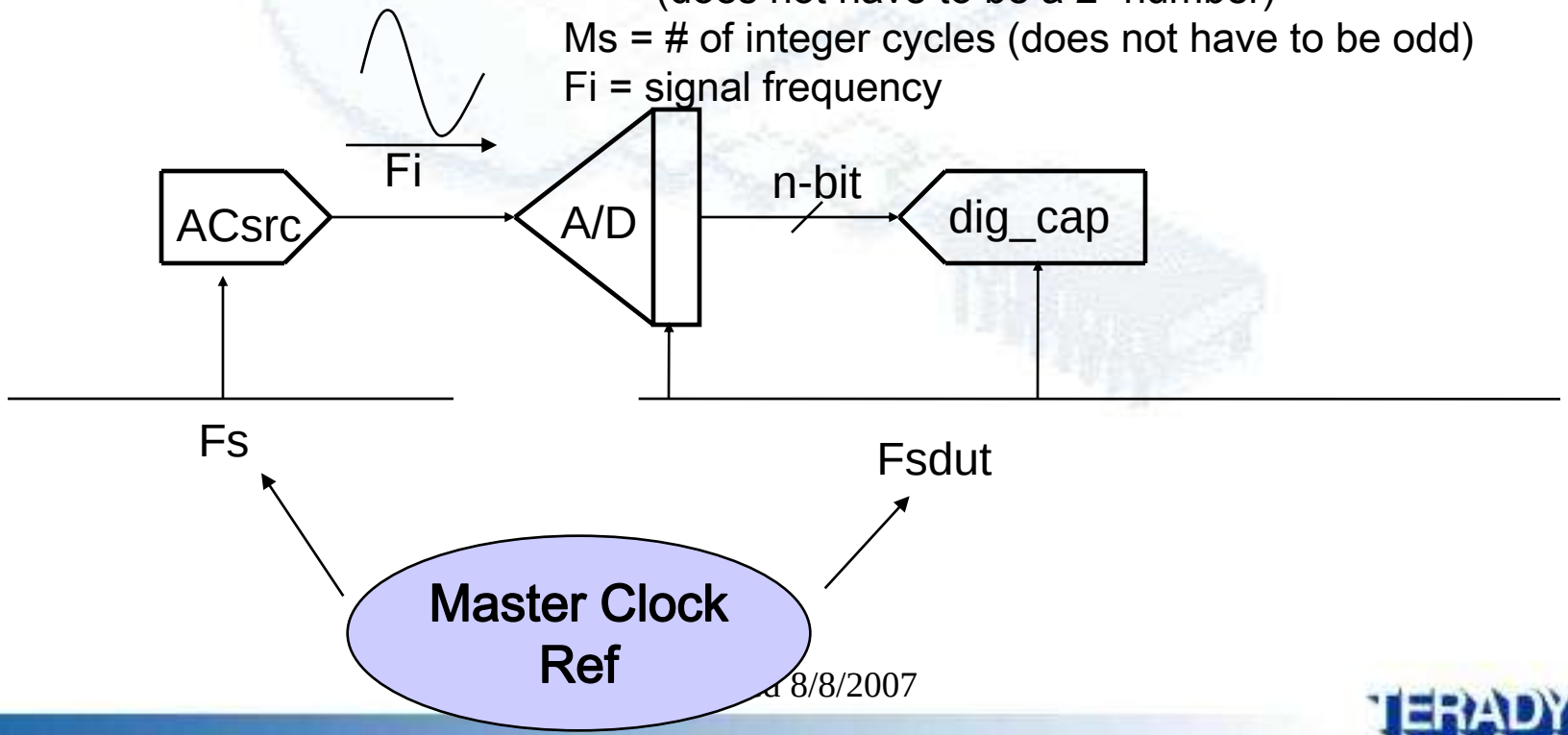


ADC DYNAMIC TEST METHODOLOGY

For AC source:

$$\frac{Fs}{Fi} = \frac{Ns}{Ms}$$

where,
Fs = AC src sampling rate
Ns = # of samples in src mem
(does not have to be a 2^x number)
Ms = # of integer cycles (does not have to be odd)
Fi = signal frequency



ADC DYNAMIC TEST METHODOLOGY

Dynamic tests: Signal to Noise Ratio (SNR)
Total Harmonic Distortion (THD)
Signal to Noise+Harmonics ratio (SINAD)

The ADC has a theoretical best ever SNR of:

SNR = (6.02N + 1.76) dB, where N= number of ADC bits.

Example: Theoretical SNR of a **10** bit ADC is:

(6.02x**10** + 1.76) ~ 62 dB.

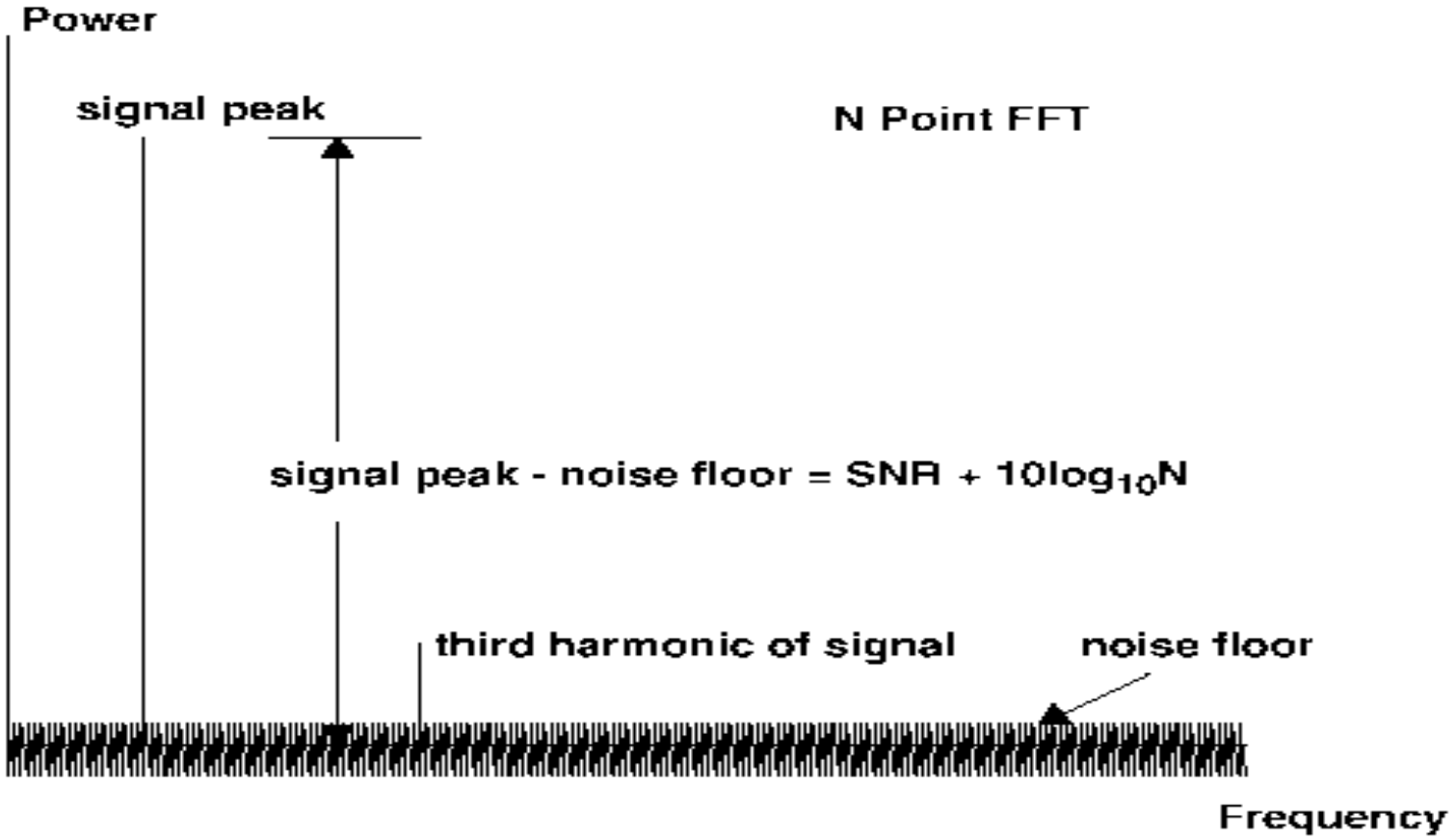
ADC DYNAMIC TEST METHODOLOGY

Dynamic ADC tests requirements:

- Resolution of ACsrc should be at least 2 to 4 bits better than DUT
- Capture MUST be coherent
- Larger Ncap size improves SNR measurement by lowering the noise floor of captured spectrum
- Noise floor of AC src MUST be lower than measured noise floor.
- Higher Fsdut and utilizing a smaller spectrum bandwidth for measurements improves SNR results.

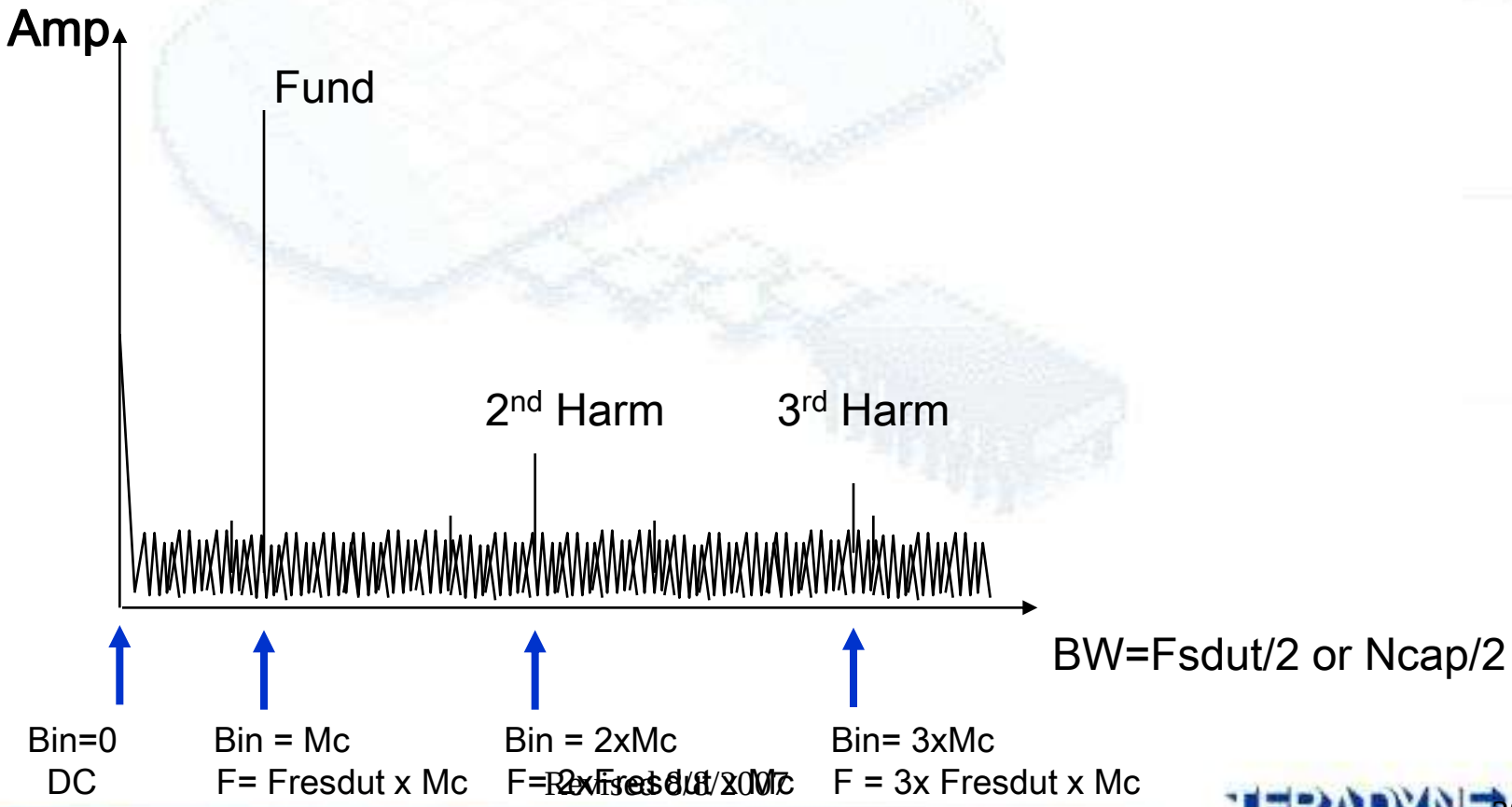
ADC DYNAMIC TEST METHODOLOGY

Spectrum of captured data: the more Ncap the better



ADC DYNAMIC TEST METHODOLOGY

ADC capture spectrum analysis: fundamental is at Bin=Mc.
Fi = (Fsdut/Ncap) x Mc = Fresdut x Mc.

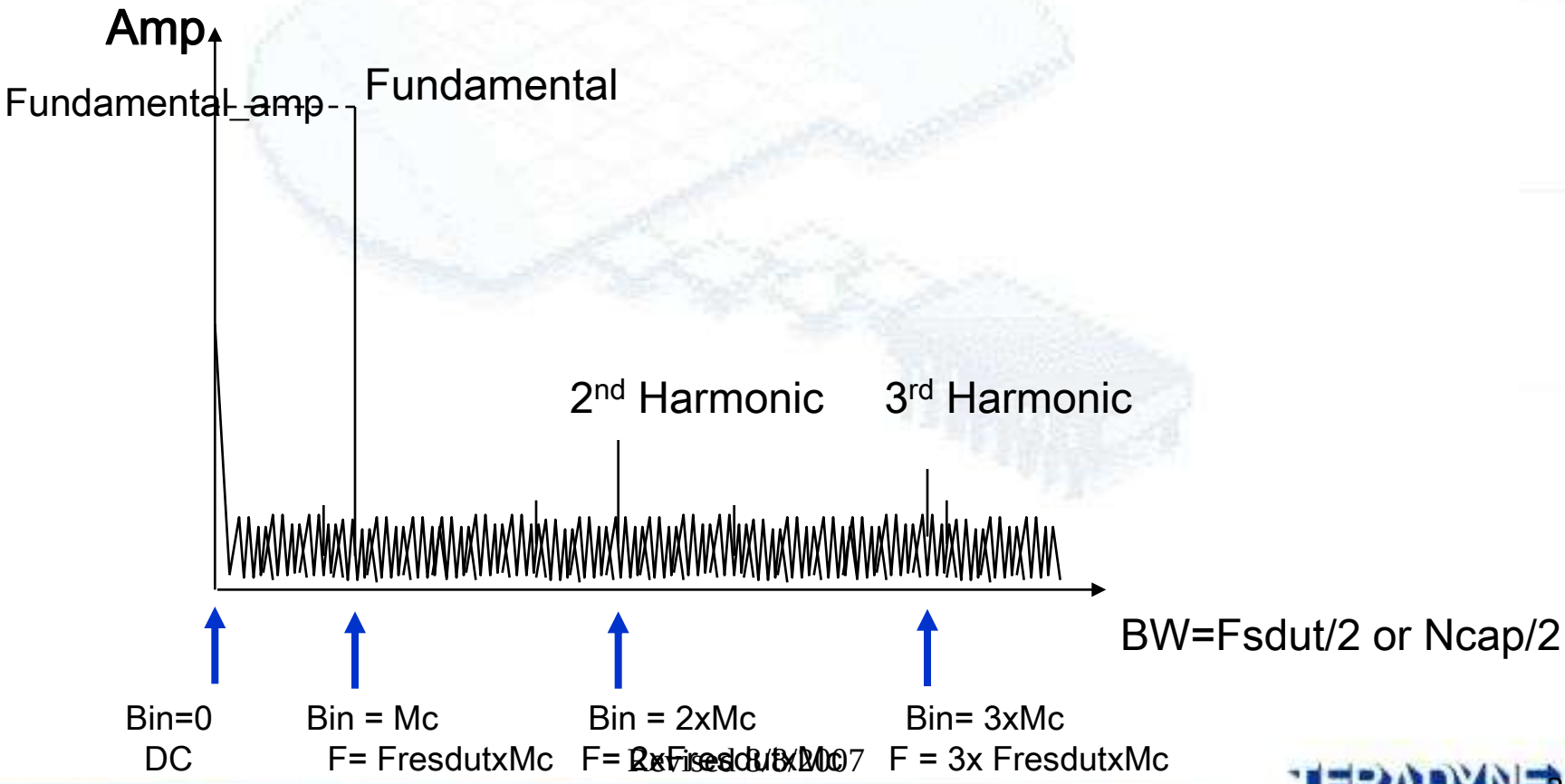


ADC DYNAMIC TEST METHODOLOGY

SNR, THD, SINAD tests:

Step 1. Store Fund Bin amplitude:

➔ Fundamental_amp.

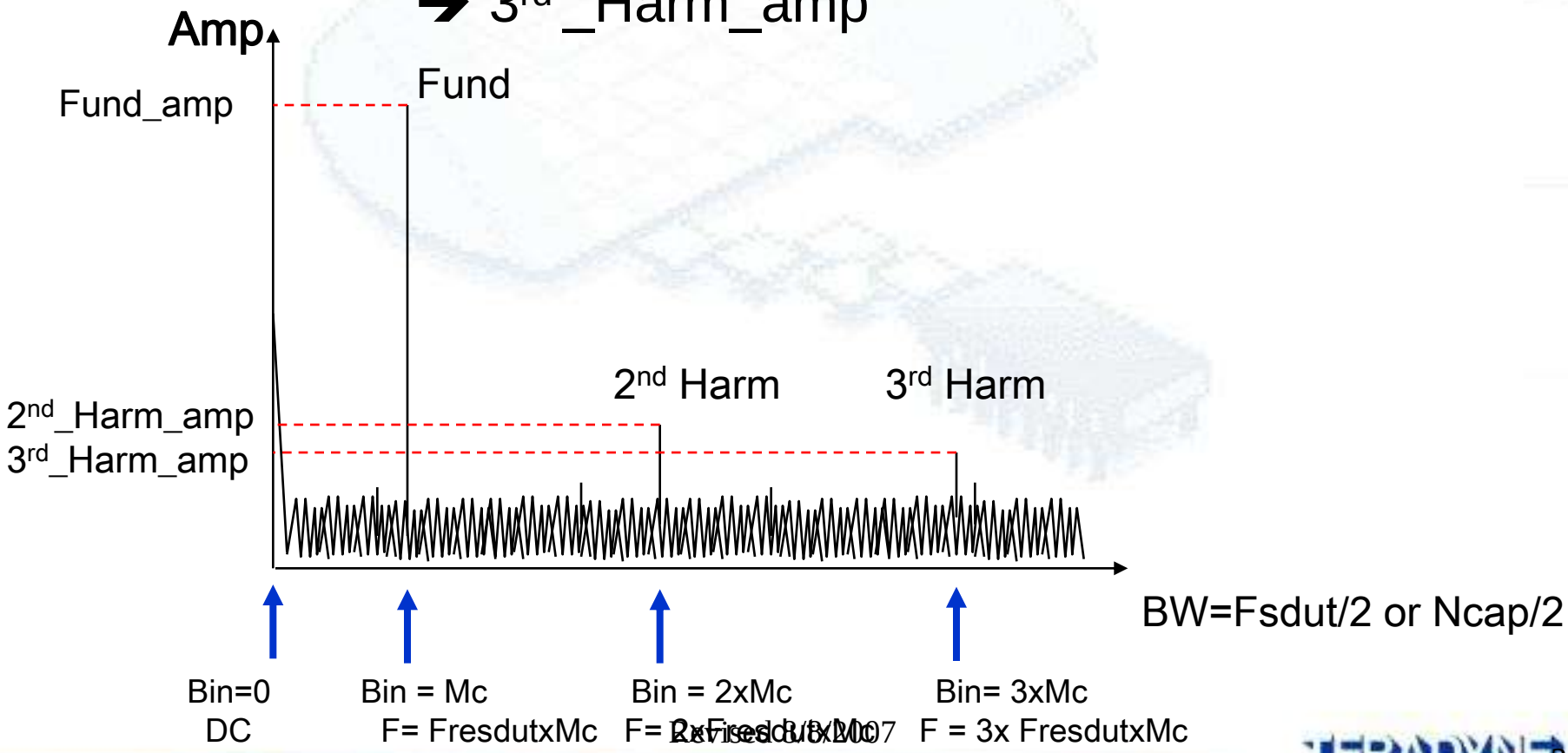


ADC DYNAMIC TEST METHODOLOGY

SNR, THD, SINAD tests:

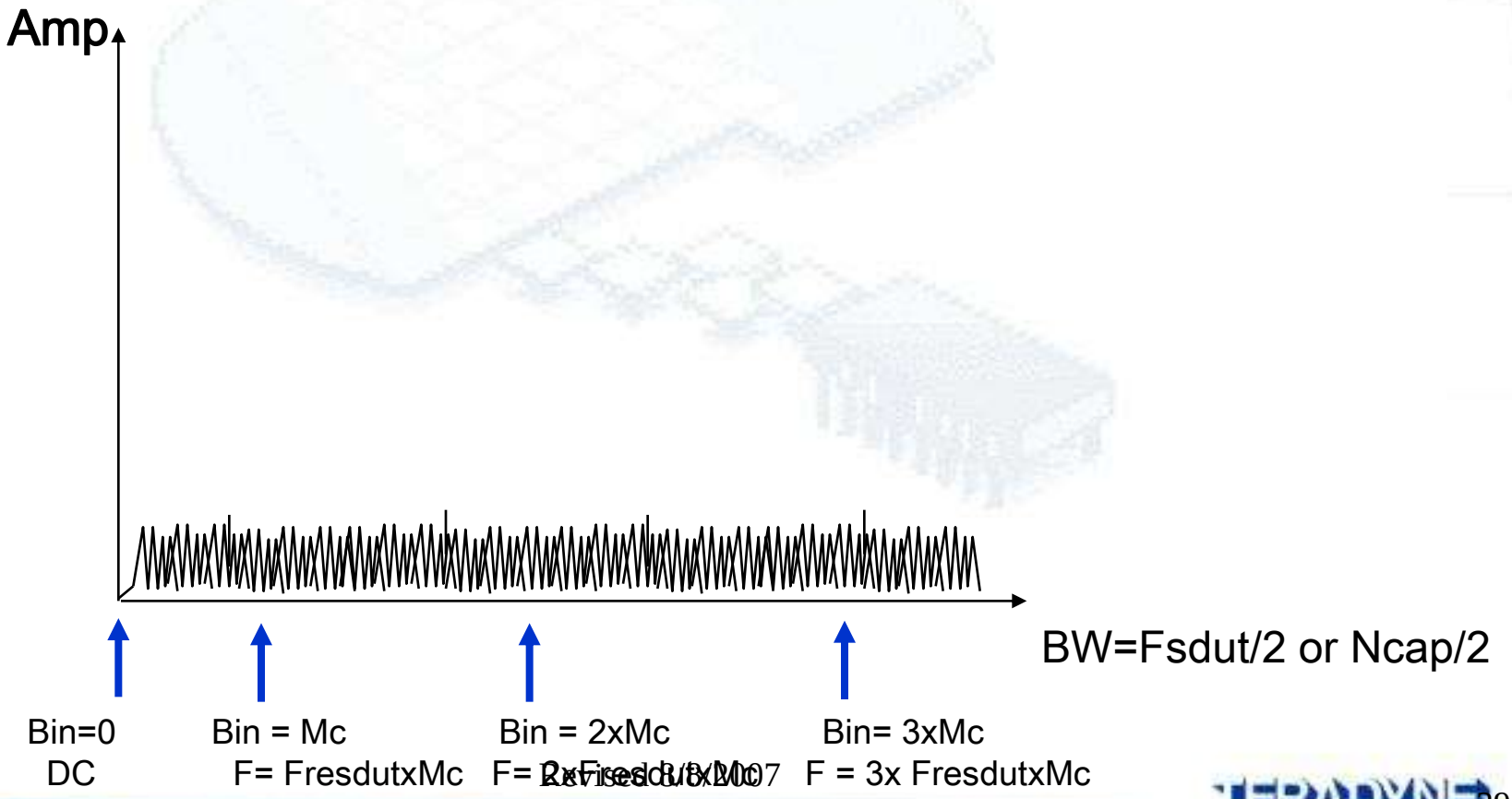
Step 2. Store 2nd and 3rd Harmonic amplitudes:

- ➔ 2nd_Harm_amp
- ➔ 3rd _Harm_amp



ADC DYNAMIC TEST METHODOLOGY

SNR, THD, SINAD tests:
Step 3. Zero out the DC,Fund and Harmonics:

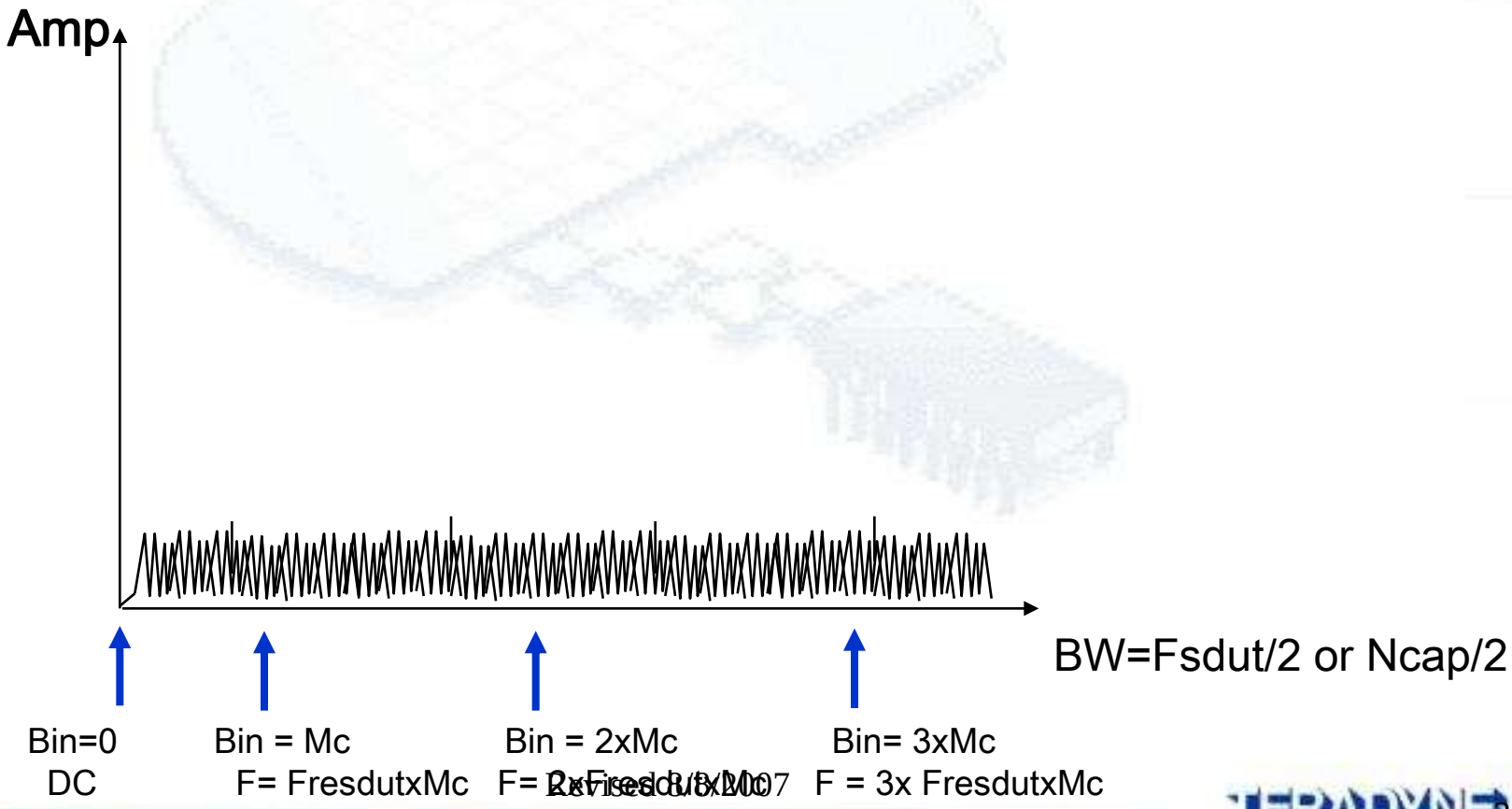


ADC DYNAMIC TEST METHODOLOGY

SNR, THD, SINAD tests:

Step 4. Sum all remaining Bins. Store results as Noise

➔ Noise_amp



ADC DYNAMIC TEST METHODOLOGY

SNR, THD, SINAD tests:
Step 5. Compute results:

Signal-to-Noise Ratio (in dB)

$= 10\log [(\text{Fund\_amp})/(\text{Noise\_amp})]$

Total Harmonic Distortion (in dB)

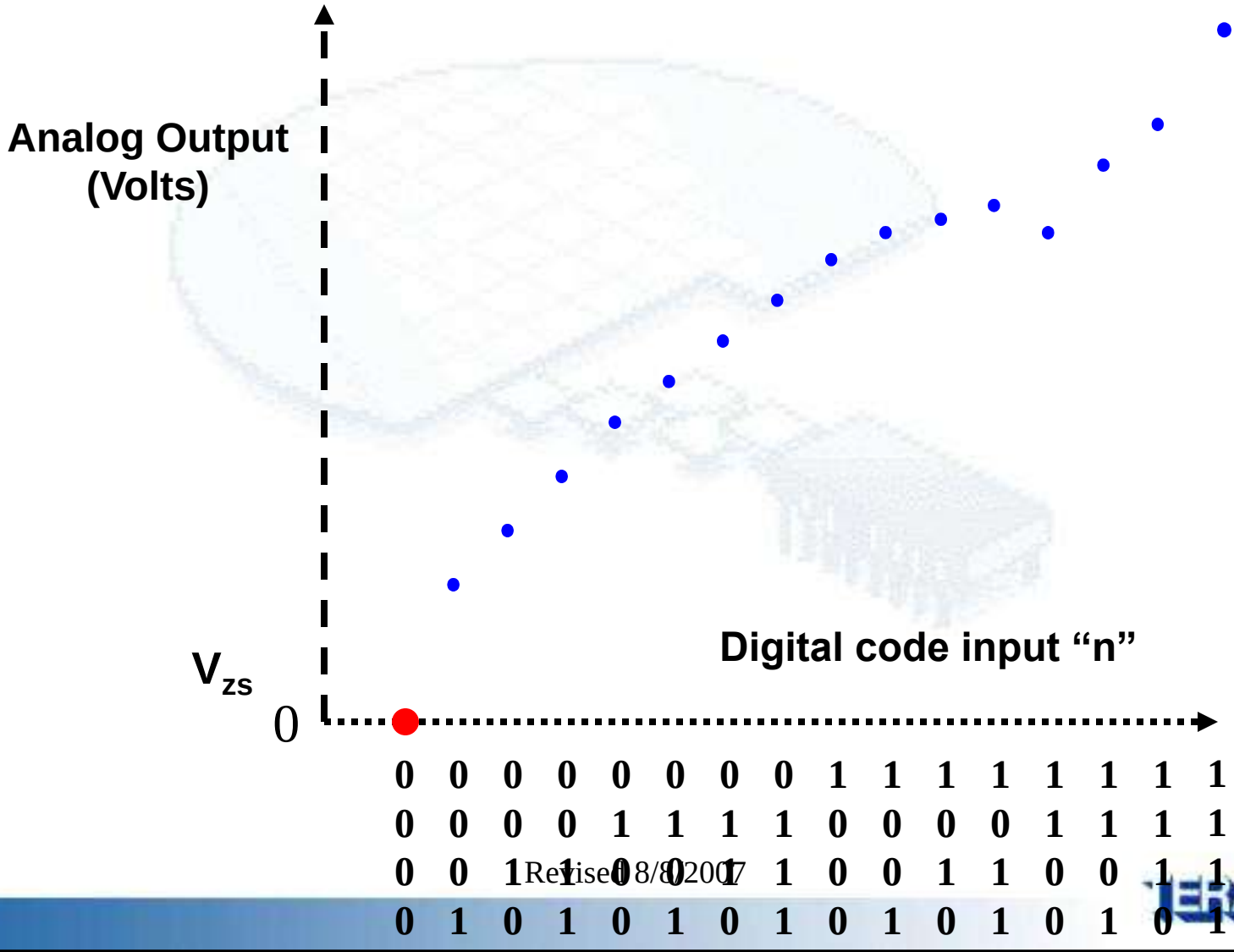
$= 10\log[(2^{nd}\text{\_Harm\_amp} + 3^{rd}\text{\_Harm\_amp})/(\text{Fund\_amp})]$

Signal-to-Noise+Distortion (in dB)

$= 10\log[(2^{nd}\text{\_Harm\_amp} + 3^{rd}\text{\_Harm\_amp} + \text{Noise\_amp})/(\text{Fund\_amp})]$

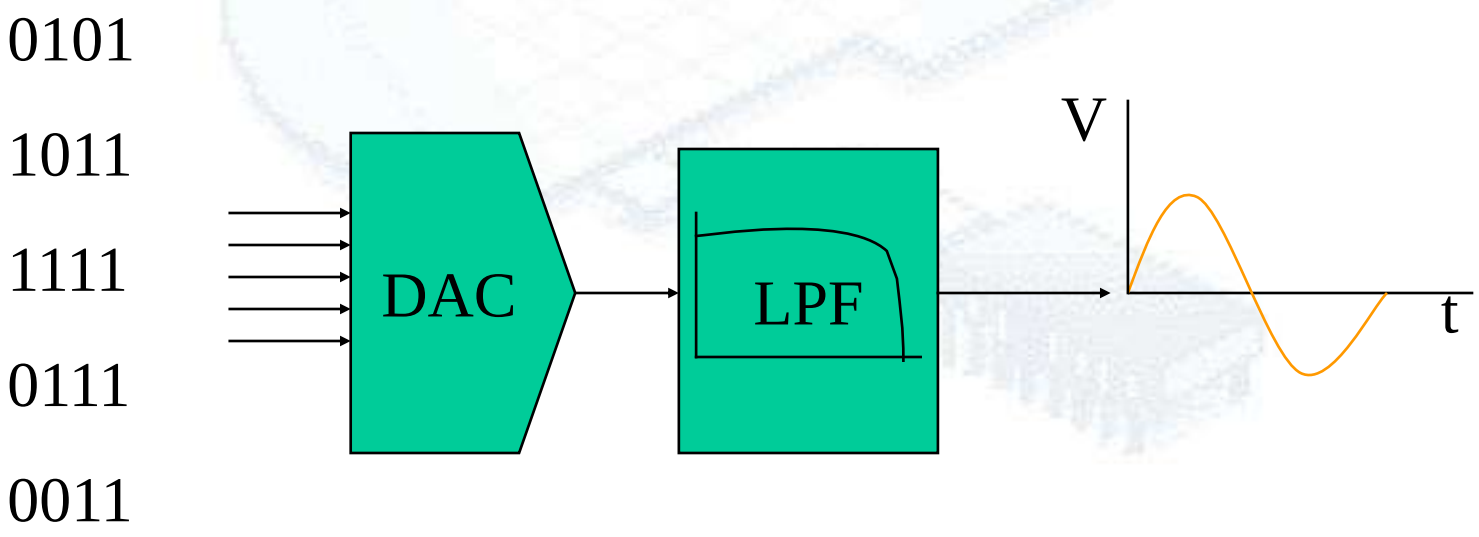
DAC TESTING

Digital-to-Analog Converter

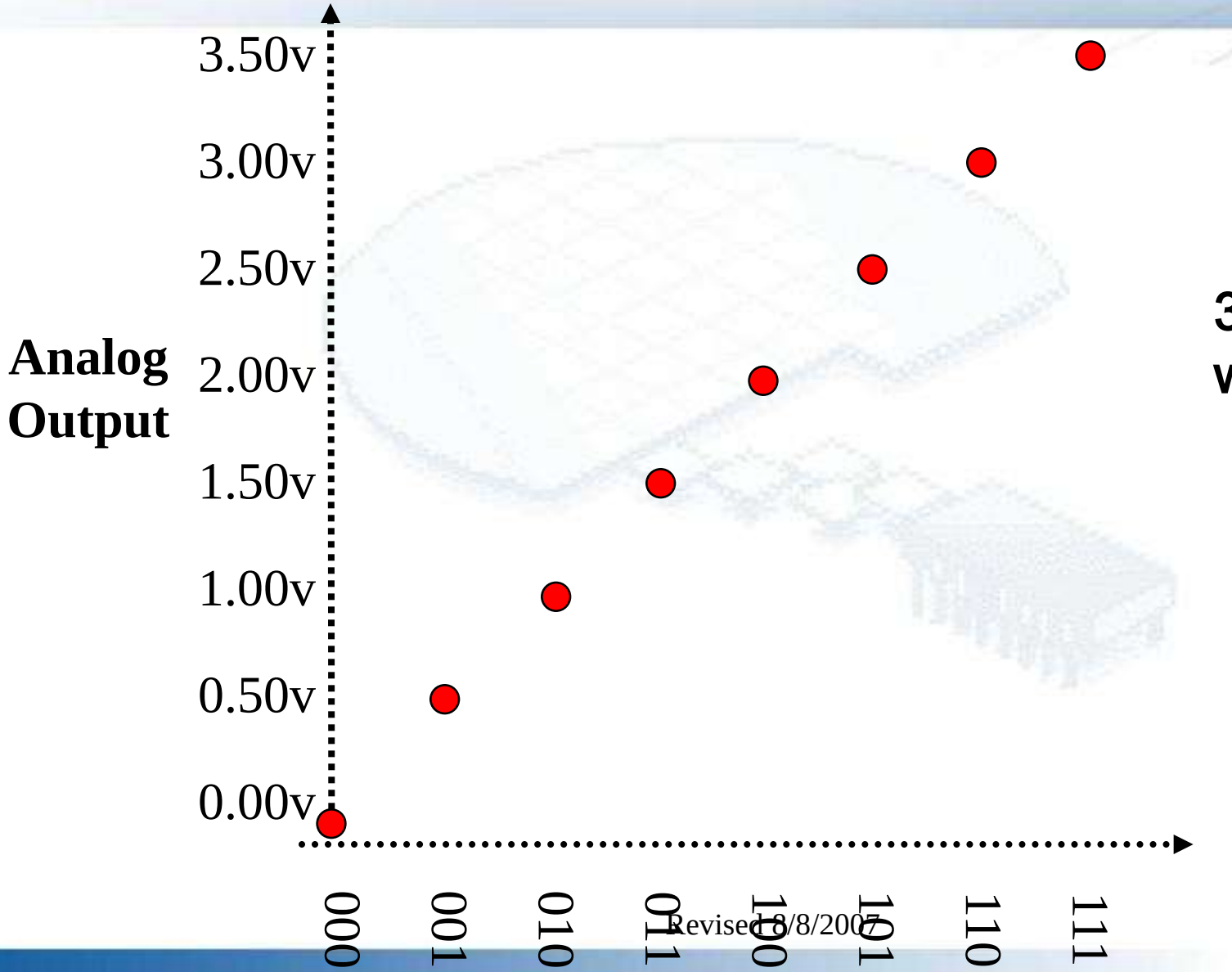


Digital-to-Analog Converter

A DAC is used to convert digital data to analog signal



Digital-to-Analog Converter

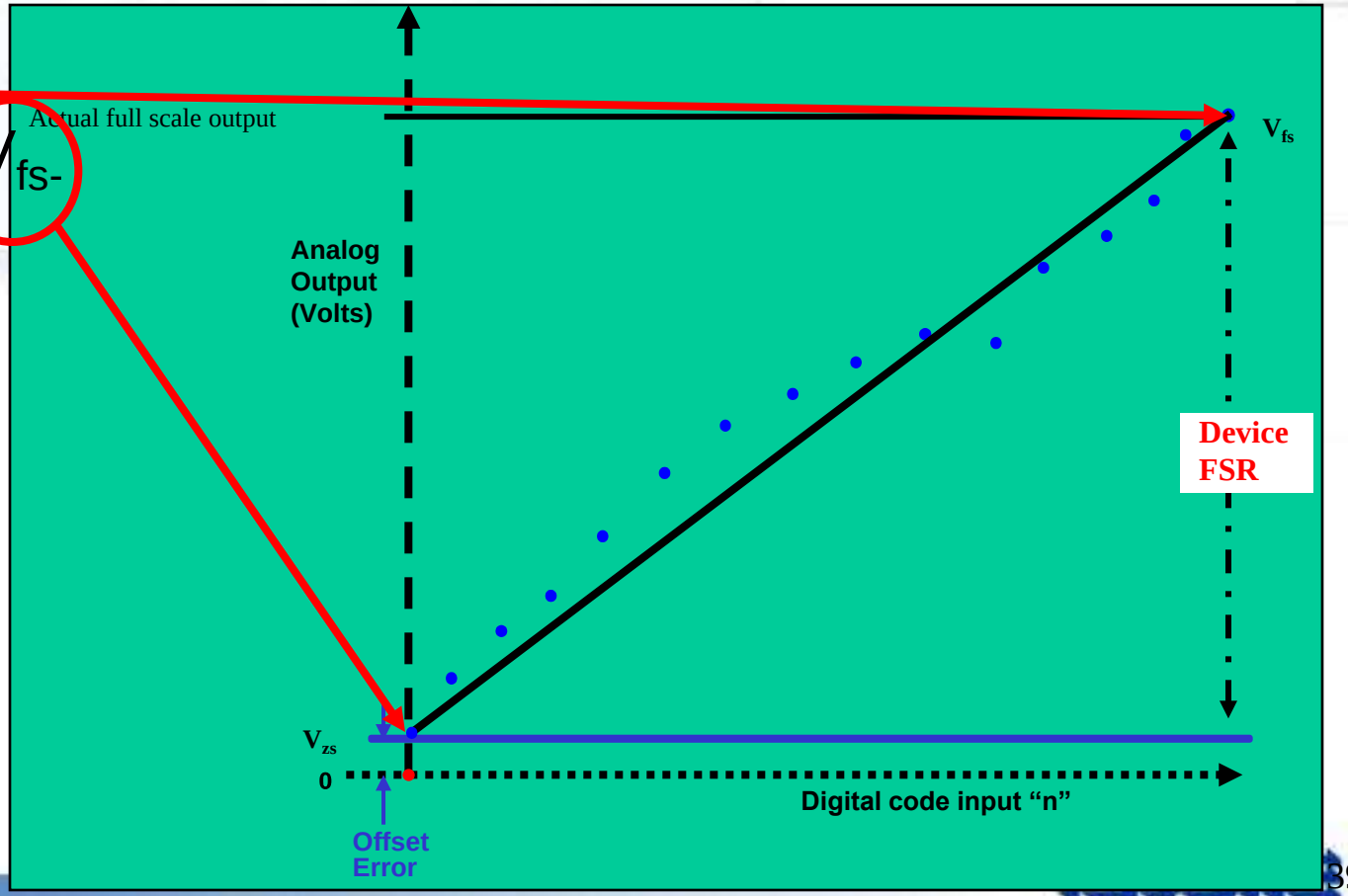


3 bit DAC
with 3.5v Ref

DAC Static Parameters

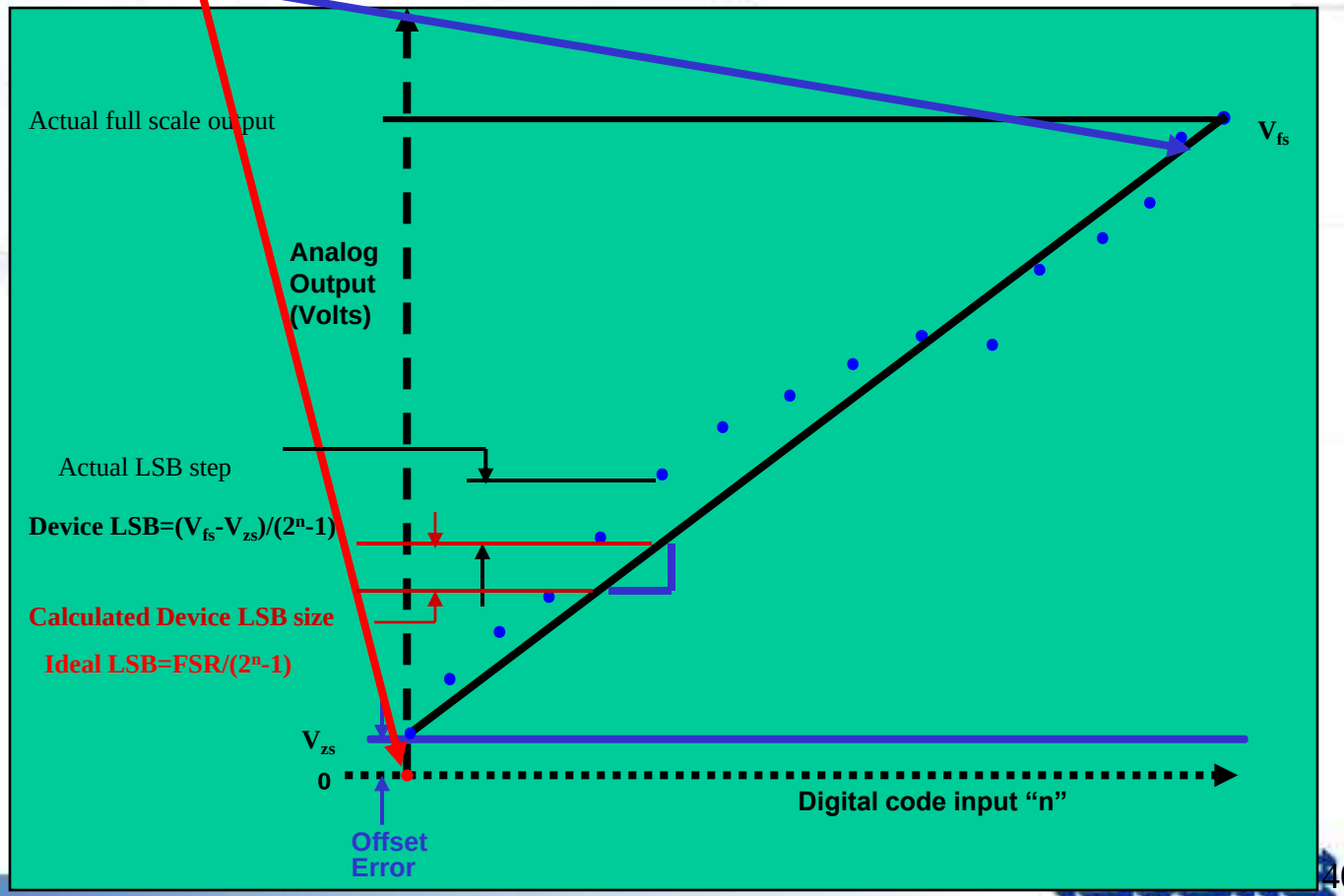
FSR - **Full Scale Range** is defined as the difference between the minimum and maximum voltages of a DAC output.

- $V_{fsr} = V_{fs+} - V_{fs-}$



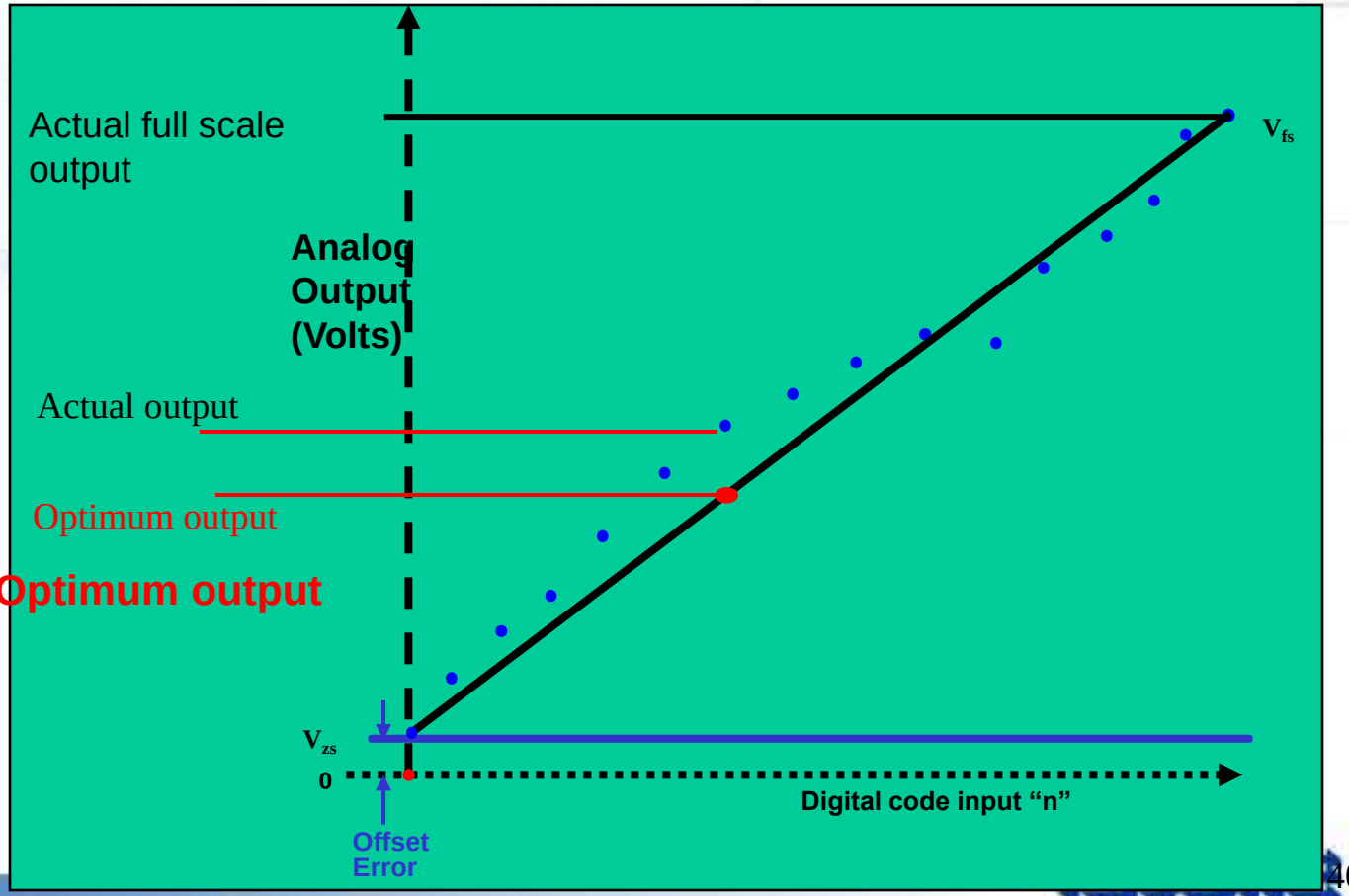
DAC Static Parameters

- $LSB_{calculated} = FSR/(2^n-1)$
- $LSB_{Device} = (V_{fs} - V_{zs})/(2^n-1)$



DAC Static Parameters

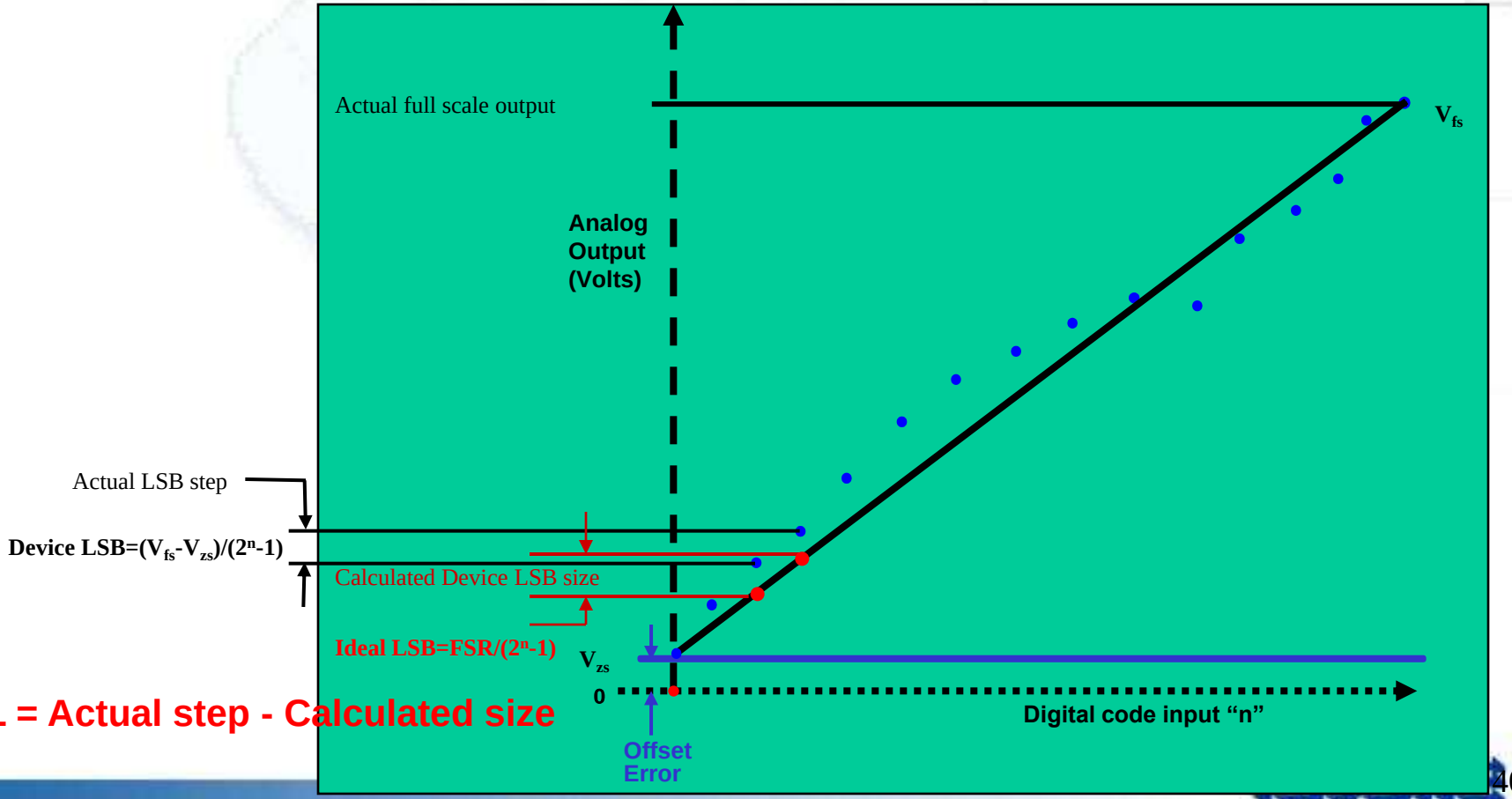
- INL = V_{actual} - V_{ideal} at a given point



INL = Actual output - Optimum output

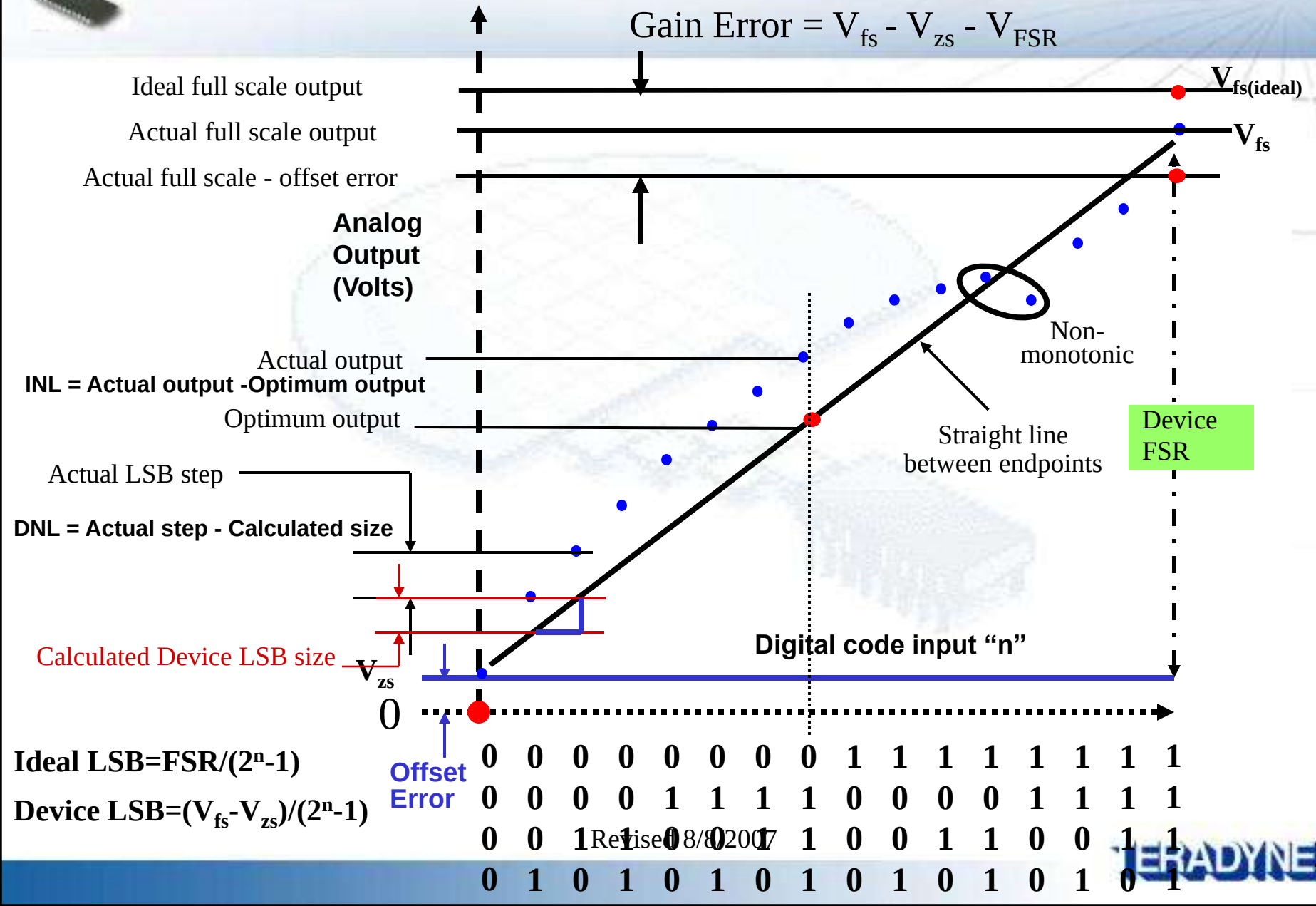
DAC Static Parameters

- DNL = LSB_{actual} - $LSB_{calculated}$ at a given point



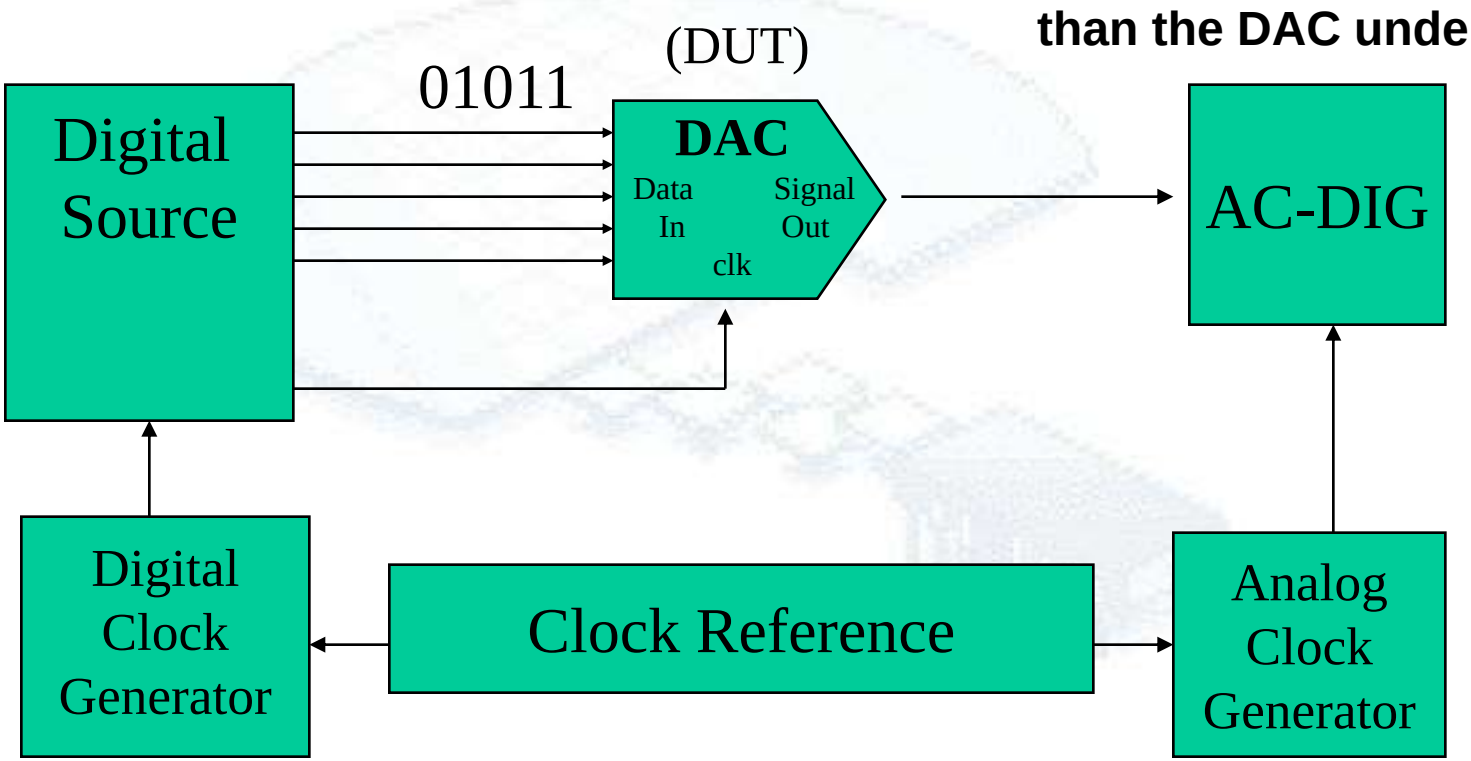
DNL = Actual step - Calculated size

DAC ERRORS


Gain Error = V_{fs} - V_{zs} - V_{FSR}
Ideal full scale output
Actual full scale output
Actual full scale - offset error
$V_{fs(ideal)}$
V_{fs}
Analog Output (Volts)
Actual output
INL = Actual output -Optimum output
Optimum output
Non-monotonic
Straight line between endpoints
Device FSR
Actual LSB step
DNL = Actual step - Calculated size
Calculated Device LSB size
V_{zs}
0
Digital code input "n"
Offset Error
Ideal LSB=FSR/(2^n-1)
Device LSB=(V_{fs}-V_{zs})/(2^n-1)
0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1
0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1
0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1
0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1

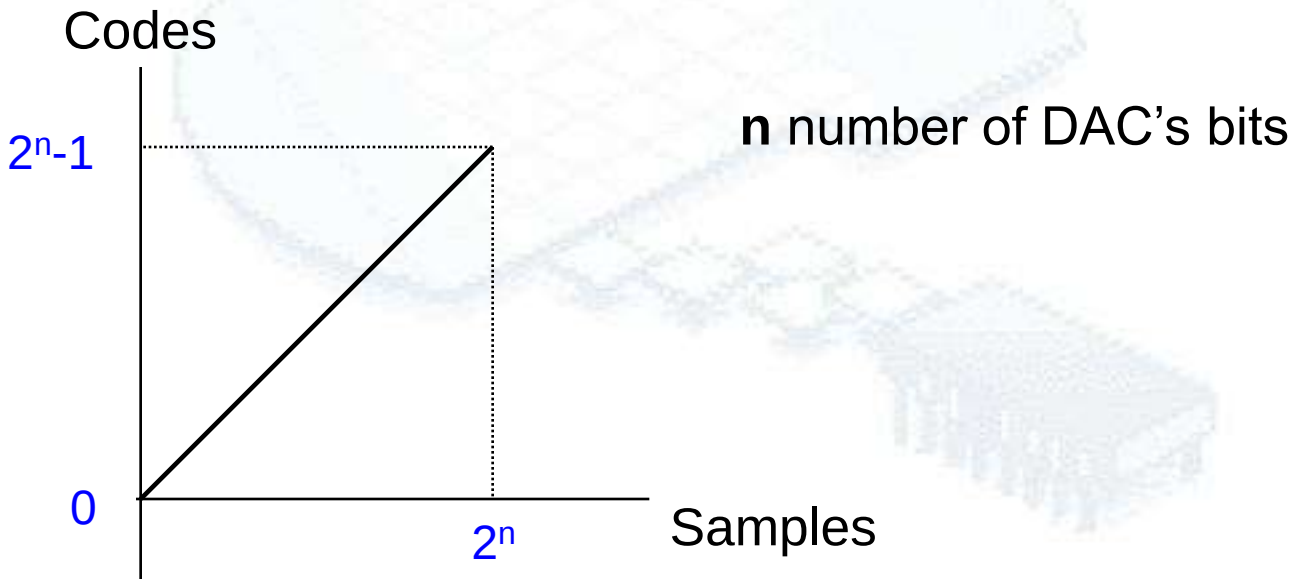
DAC TEST SETUP

AC Digitizer should be 2-4 bits more resolution than the DAC under test



DAC STATIC TEST METHODOLOGY
Ramp Method

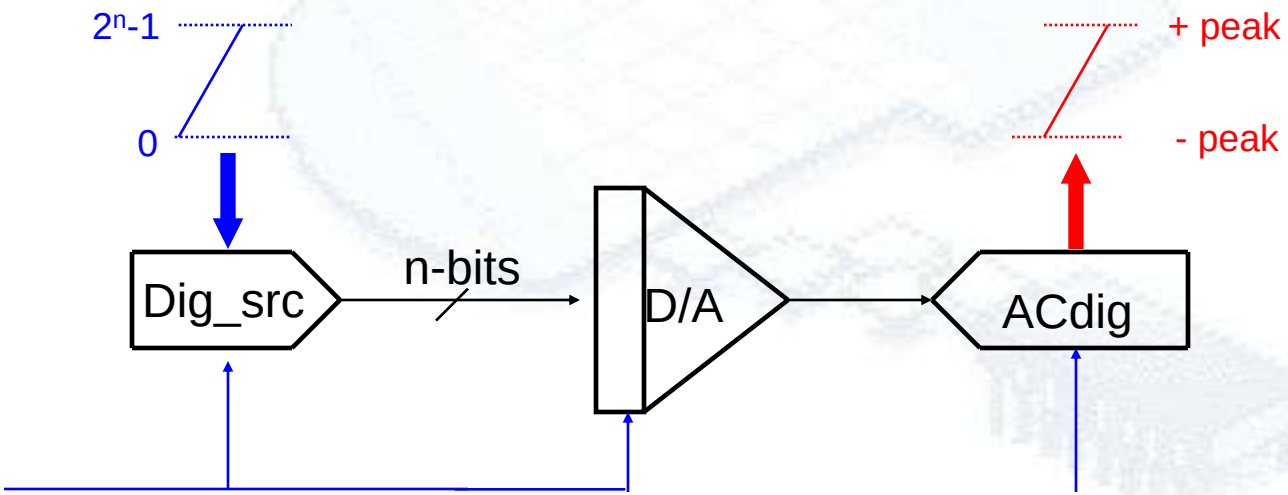
Make a ramp wave segment for dig_src (as input to DAC)



n number of DAC's bits

DAC STATIC TEST METHODOLOGY
Ramp Method

Block diagram of signal setup



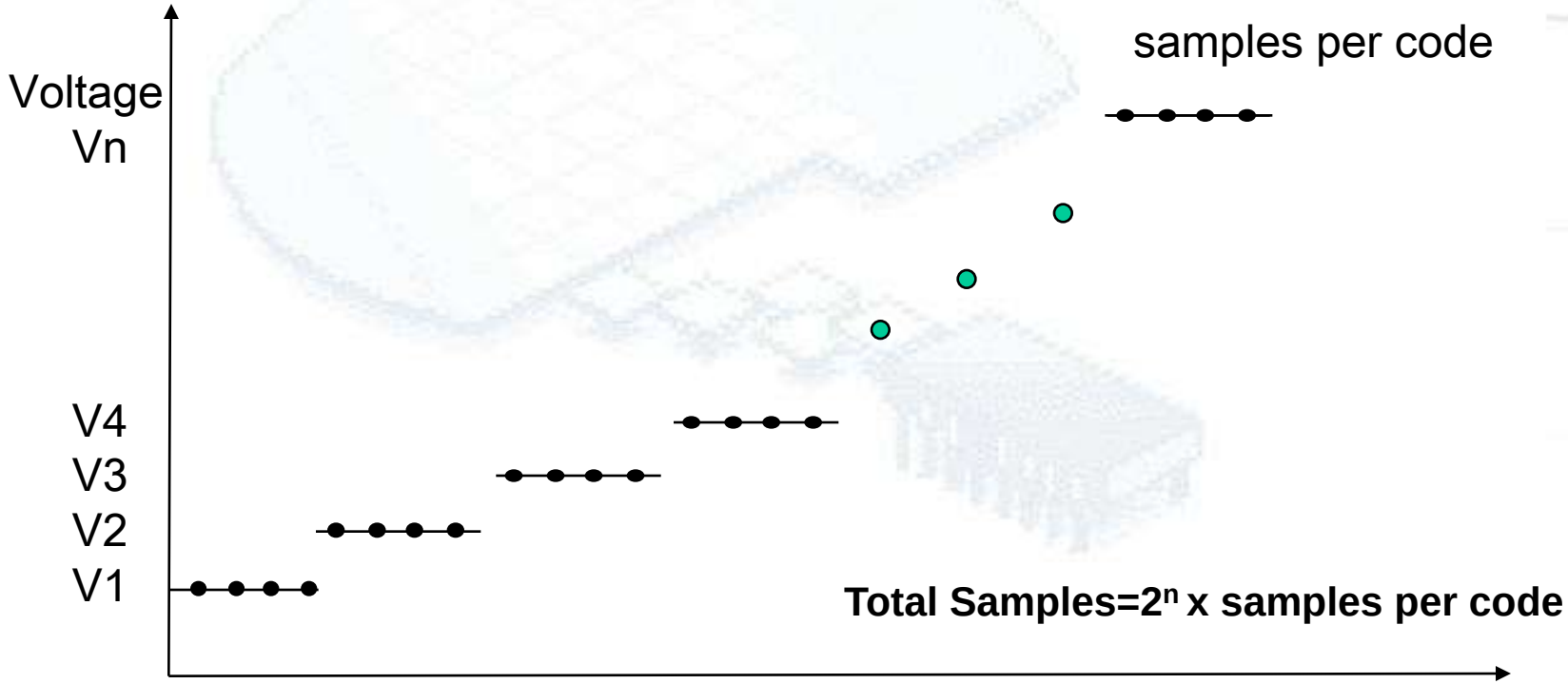
$Fs = 2^n \bullet Ramp\_freq$

$Fs = 2^n \bullet Ramp\_freq \bullet samples\_per\_code$

$Samples = Fs \times (1/Ramp\_freq)$

DAC STATIC TEST METHODOLOGY
Ramp Method

Capture output of DAC using ACdig



Captured/Digitized Ramp

Revised 8/8/2007

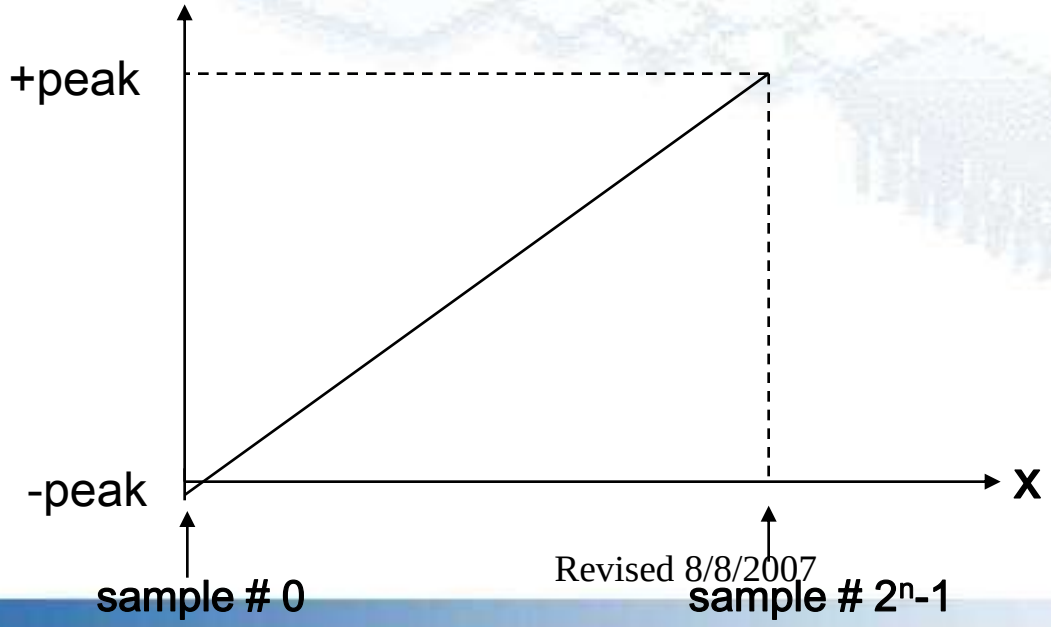
DAC STATIC TEST METHODOLOGY
Ramp Method

Calculate average LSB size to make ideal ramp

LSB = (+peak – (-peak))/ (2n – 1)

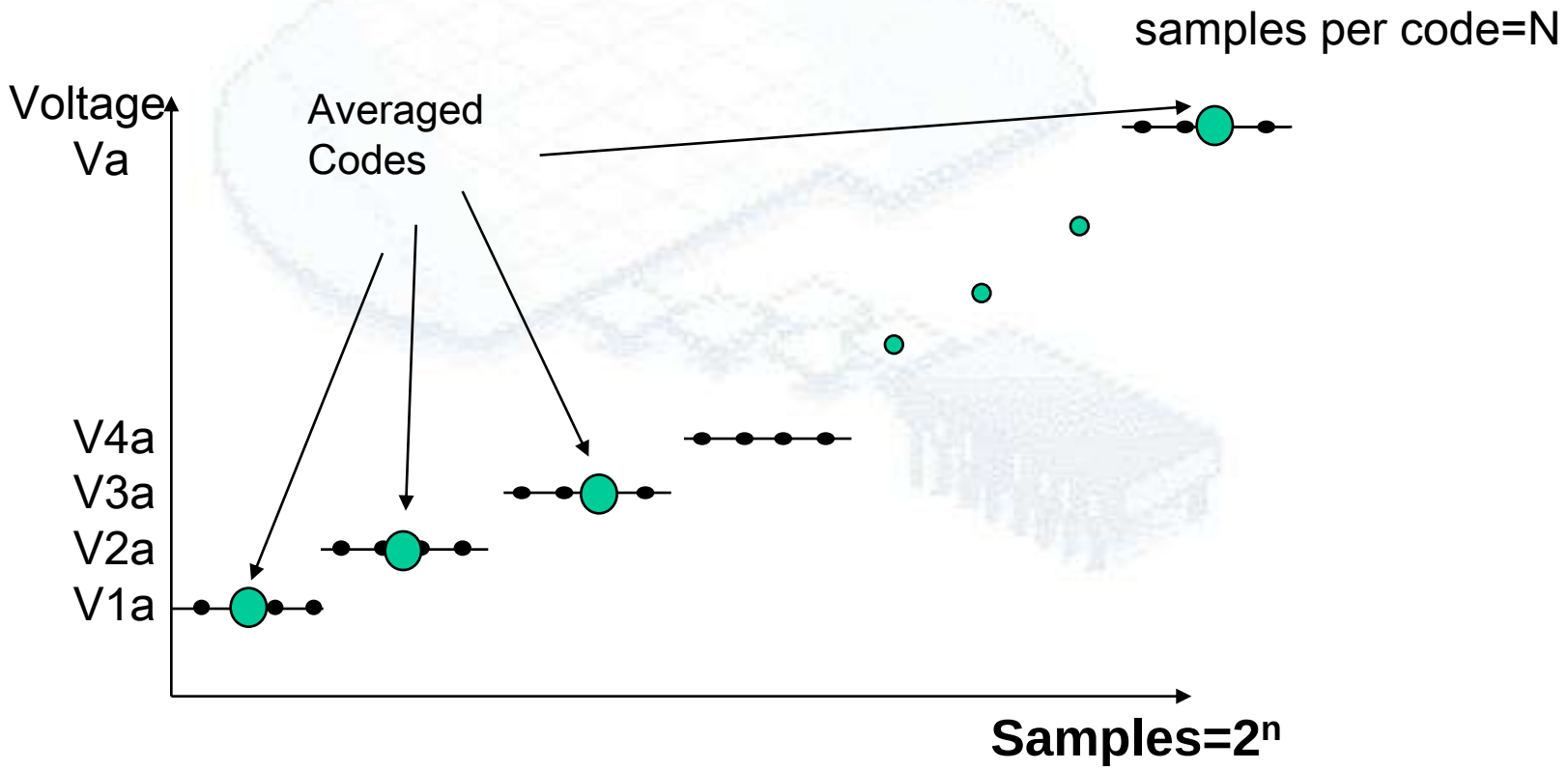
Make an ideal ramp

Ideal straight line; y=mx+c where, m= LSB and c= -peak



DAC STATIC TEST METHODOLOGY
Ramp Method

Average-out the voltage levels for each code.

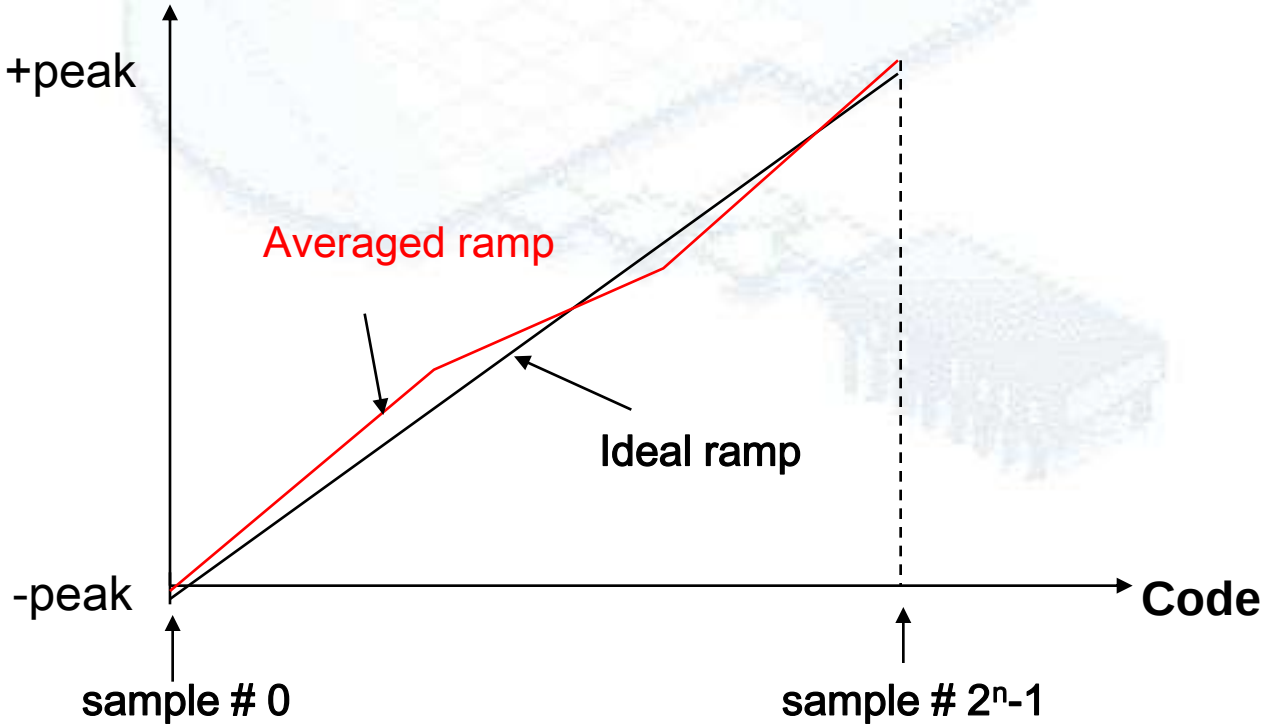


DAC STATIC TEST METHODOLOGY
Ramp Method

Calculate INL="Capture wave - ideal wave"

INL[i] = Averaged_ramp[i] – Ideal_ramp[i]

Find INLmax

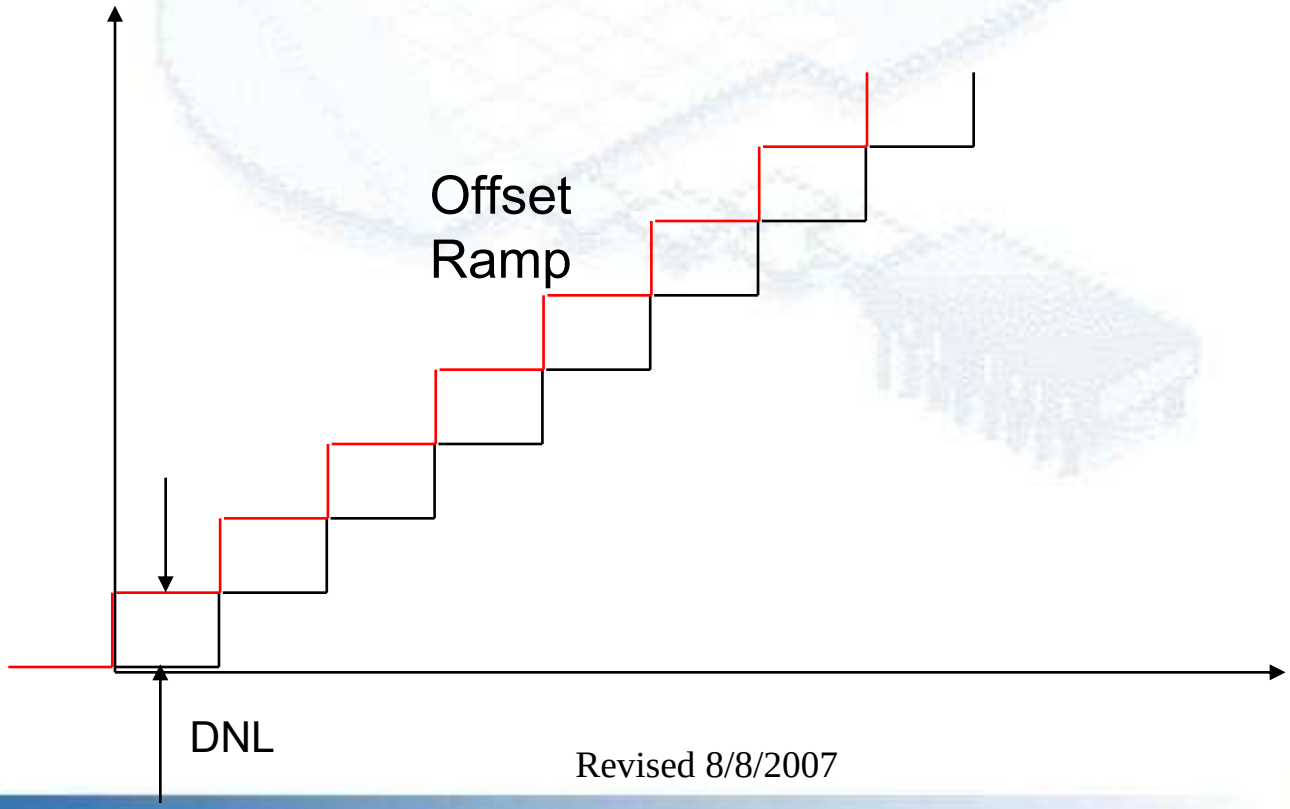


DAC STATIC TEST METHODOLOGY
Ramp Method

Calculate DNL:

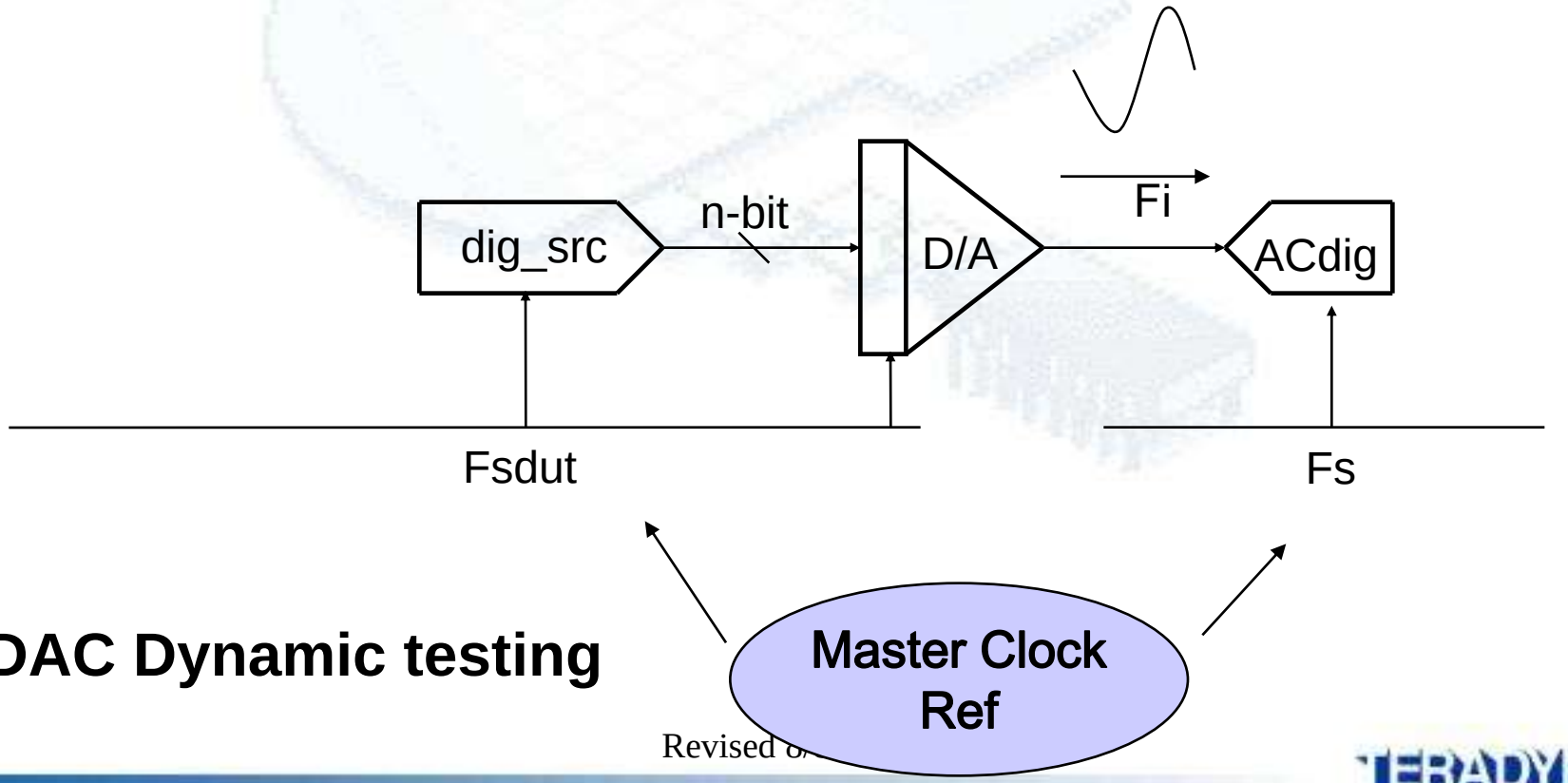
DNL[i] = Averaged_ramp[i+1] – Averaged_ramp[i]

Find DNLmax



DAC DYNAMIC TEST METHODOLOGY

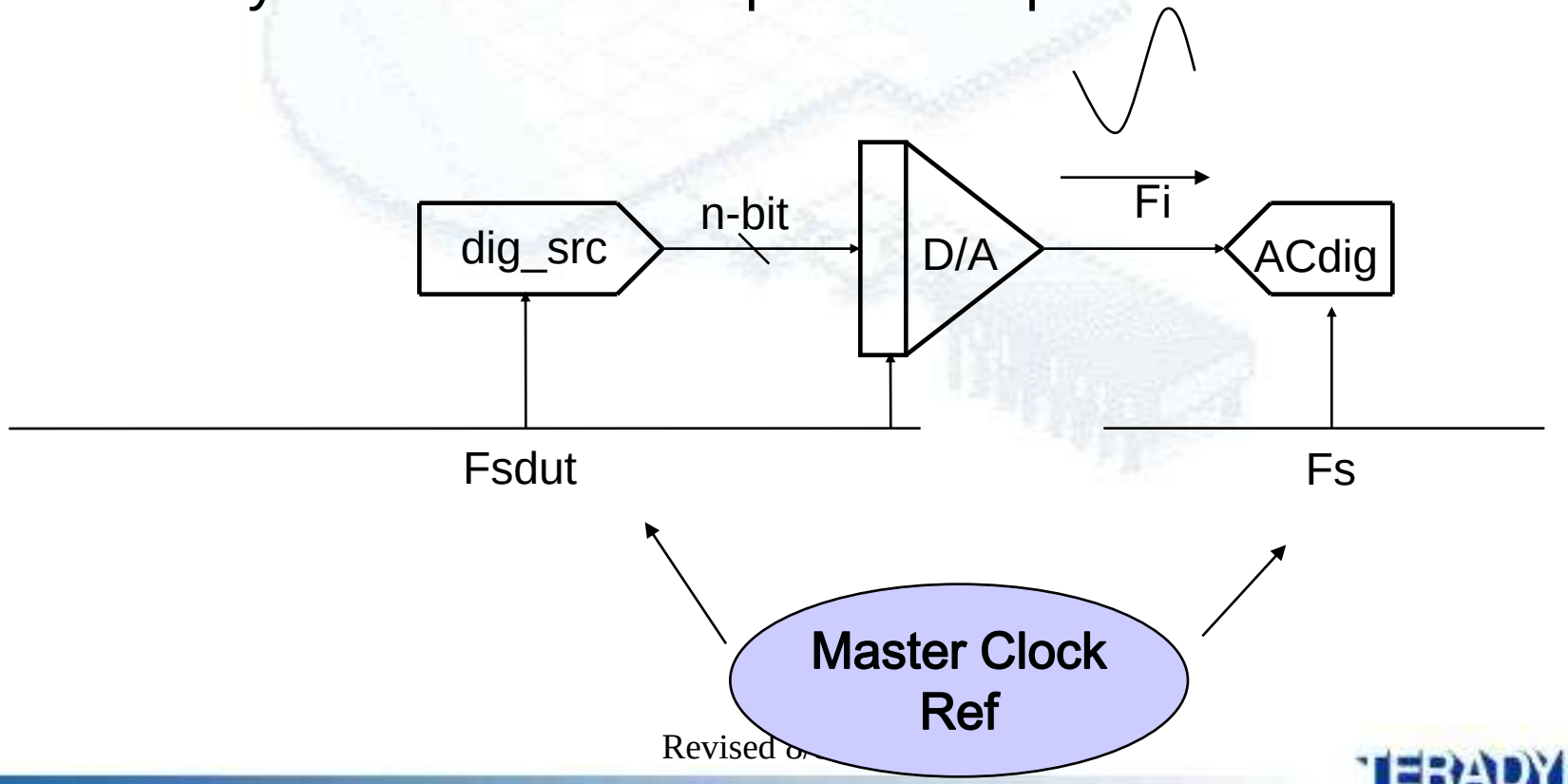
It is common practice to ensure the analog clock and the digital clock are referenced to a common master clock so that phase relationship of the clock sources are fixed and synchronized, making test results highly repeatable.



DAC Dynamic testing

DAC DYNAMIC TEST METHODOLOGY

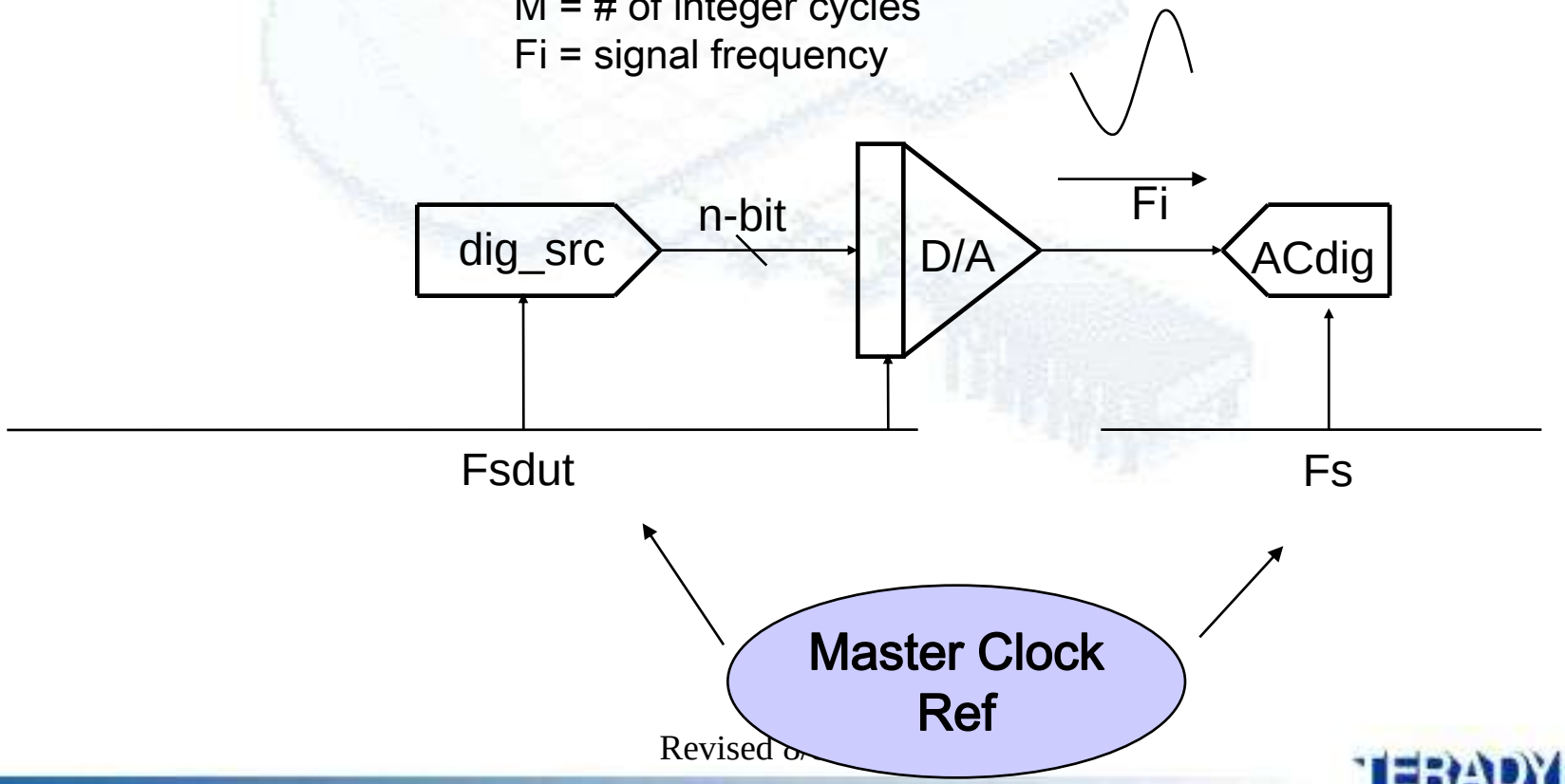
A dig_src is used to input discrete sinewave data to the DAC. The converted analog levels (sinewave) from the DAC output is digitized/ captured by the AC digitizer.
Coherency of source and capture is important.



DAC DYNAMIC TEST METHODOLOGY

For dig_src: $\frac{Fsdut}{Fi} = \frac{N}{M}$

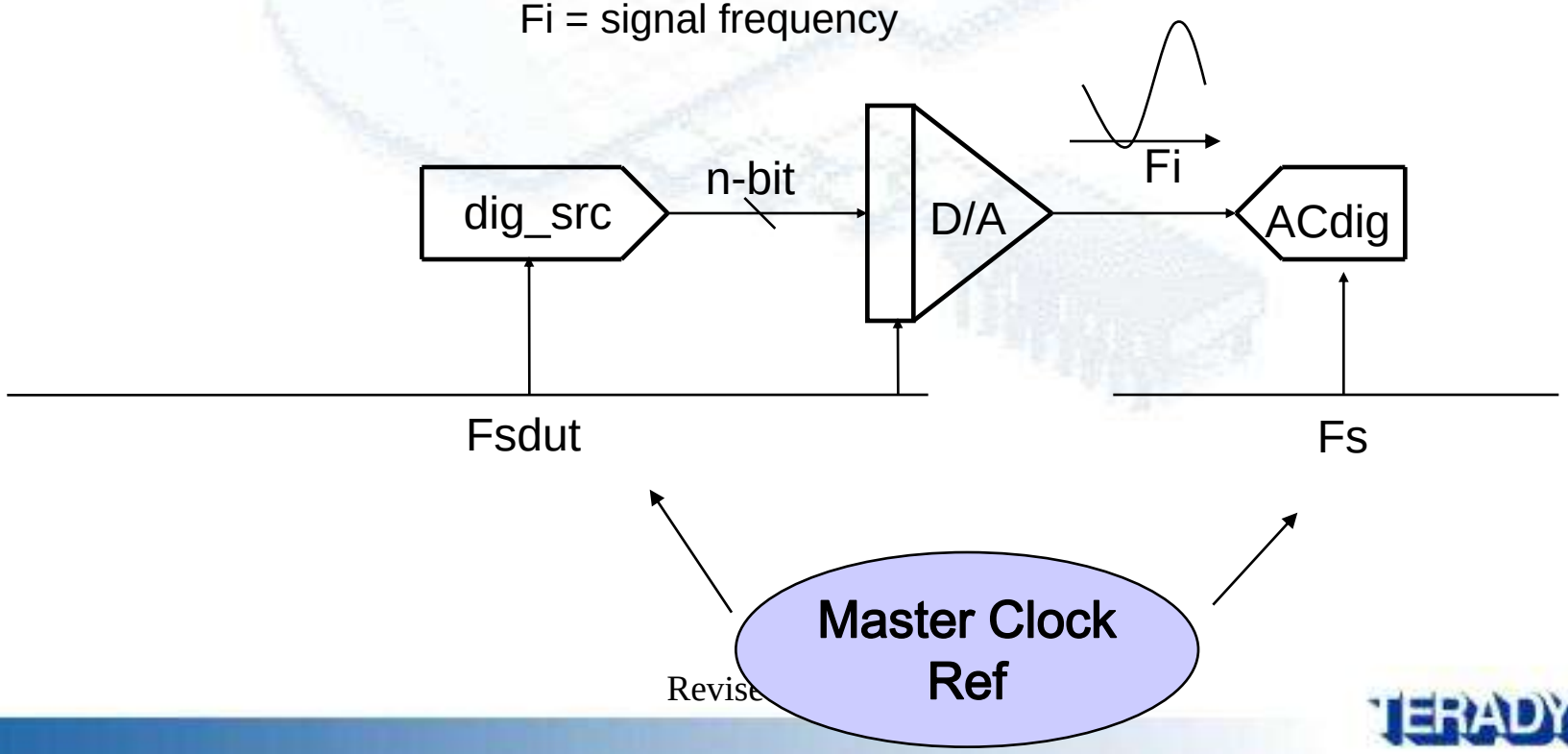
where Fsdut = DAC sampling rate= dig_src sample rate
N = # of samples stored
M = # of integer cycles
Fi = signal frequency



DAC DYNAMIC TEST METHODOLOGY

For AC digitizer: $\frac{Fs}{Fi} = \frac{Ncap}{M}$

where Fs = AC digitizer sampling rate
Ncap = # of samples in src memory
(has to be a 2^x number)
Mc = # of integer cycles (has to be odd)
Fi = signal frequency



DAC DYNAMIC TEST METHODOLOGY

Dynamic tests:

Signal to Noise Ratio (SNR)
Total Harmonic Distortion (THD)
Signal to Noise+Harmonics ratio (SINAD)

The digitizer can be thought of as an ADC device with a theoretical SNR = (6.02**N** + 1.76) dB, where **N** is the resolution of the digitizer.

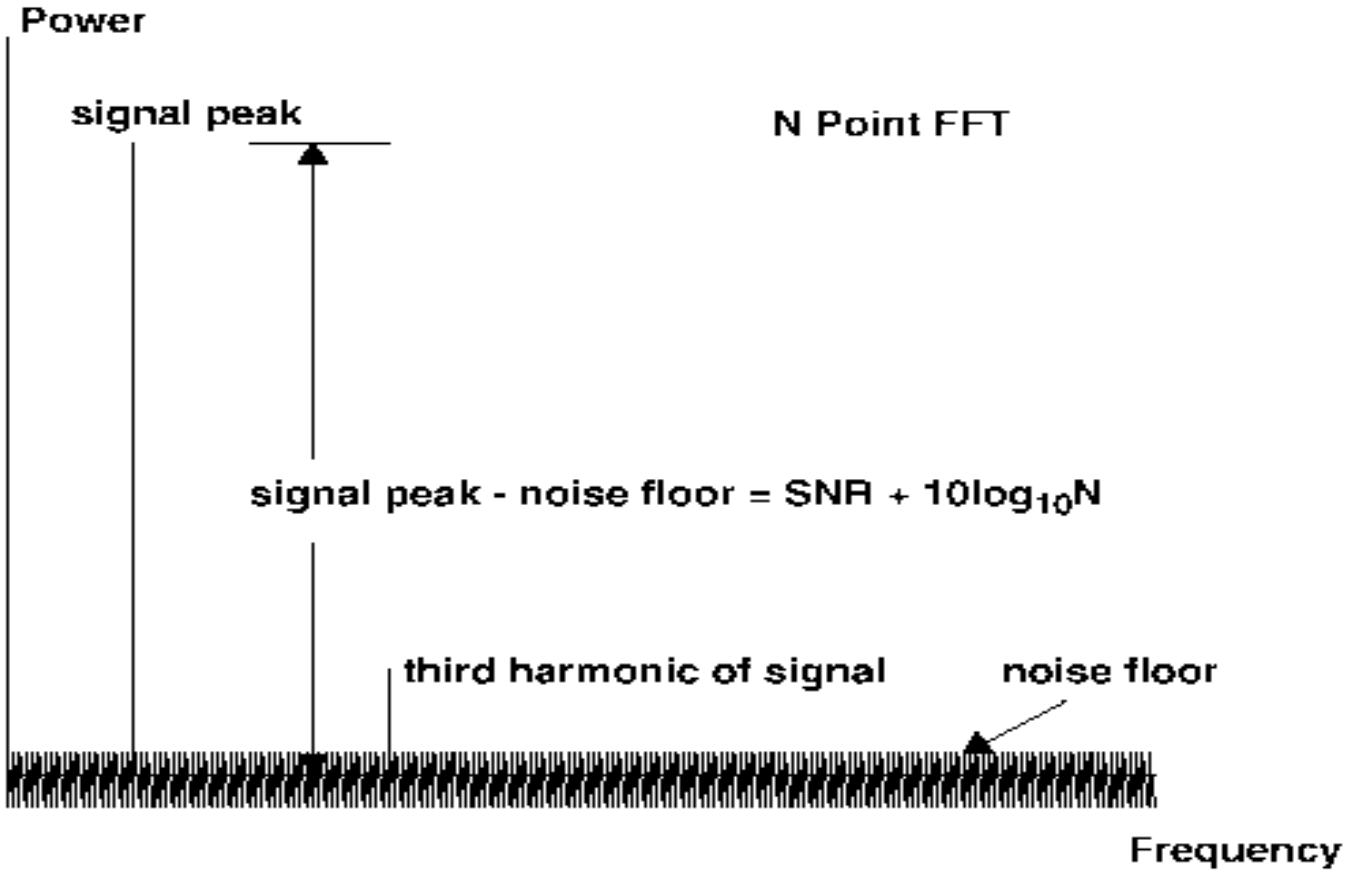
DAC DYNAMIC TEST METHODOLOGY

Dynamic DAC tests requirements:

- Resolution of AC dig must be 2 to 4 bits better than DUT
- Capture MUST be coherent
- Larger Ncap size improves SNR measurement by lowering the noise floor of captured spectrum
- Noise floor of AC digitizer **MUST** be lower than measured noise floor.
- Higher Fs and utilizing a smaller spectrum bandwidth for measurements improves SNR results.

DAC DYNAMIC TEST METHODOLOGY

Spectrum of captured data: the higher Ncap the better

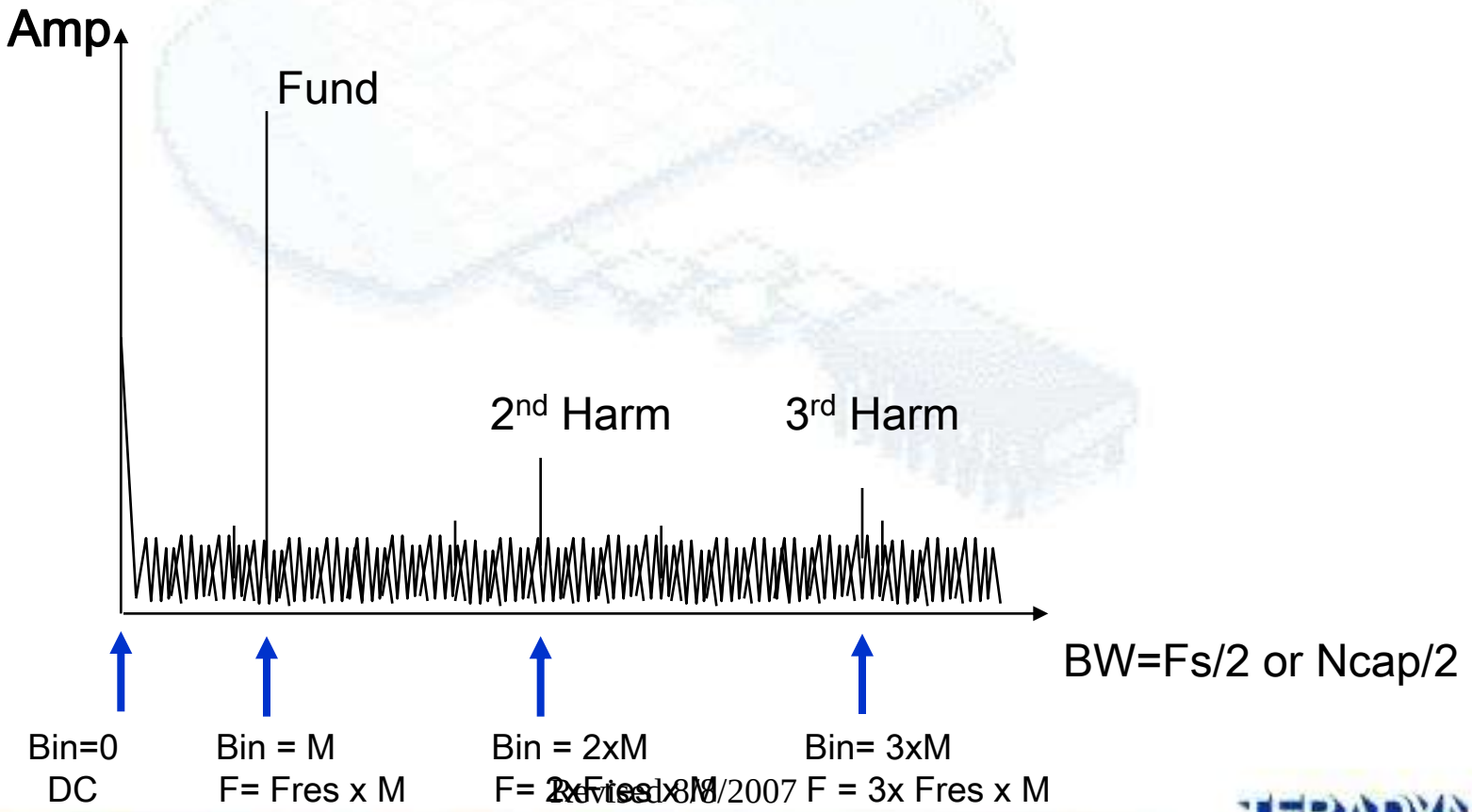


DAC DYNAMIC TEST METHODOLOGY

DAC captured-spectrum analysis:

Fundamental is at Bin=Mc.

Fi = (Fs/Ncap) x M = Fres x M

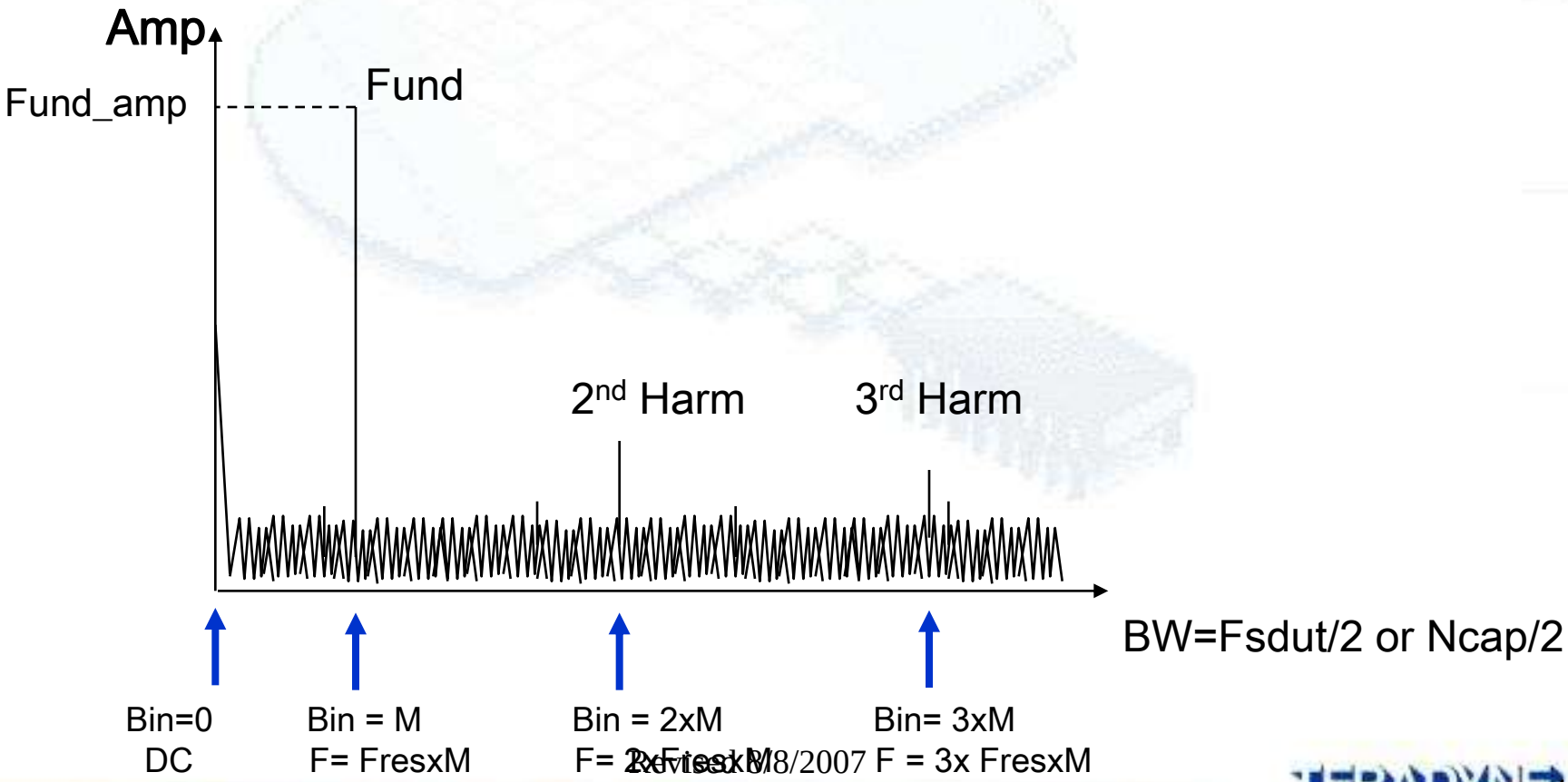


DAC DYNAMIC TEST METHODOLOGY

SNR, THD, SINAD tests:

Step 1. Store Fundamental Bin amplitude:

➔ Fund_amp.

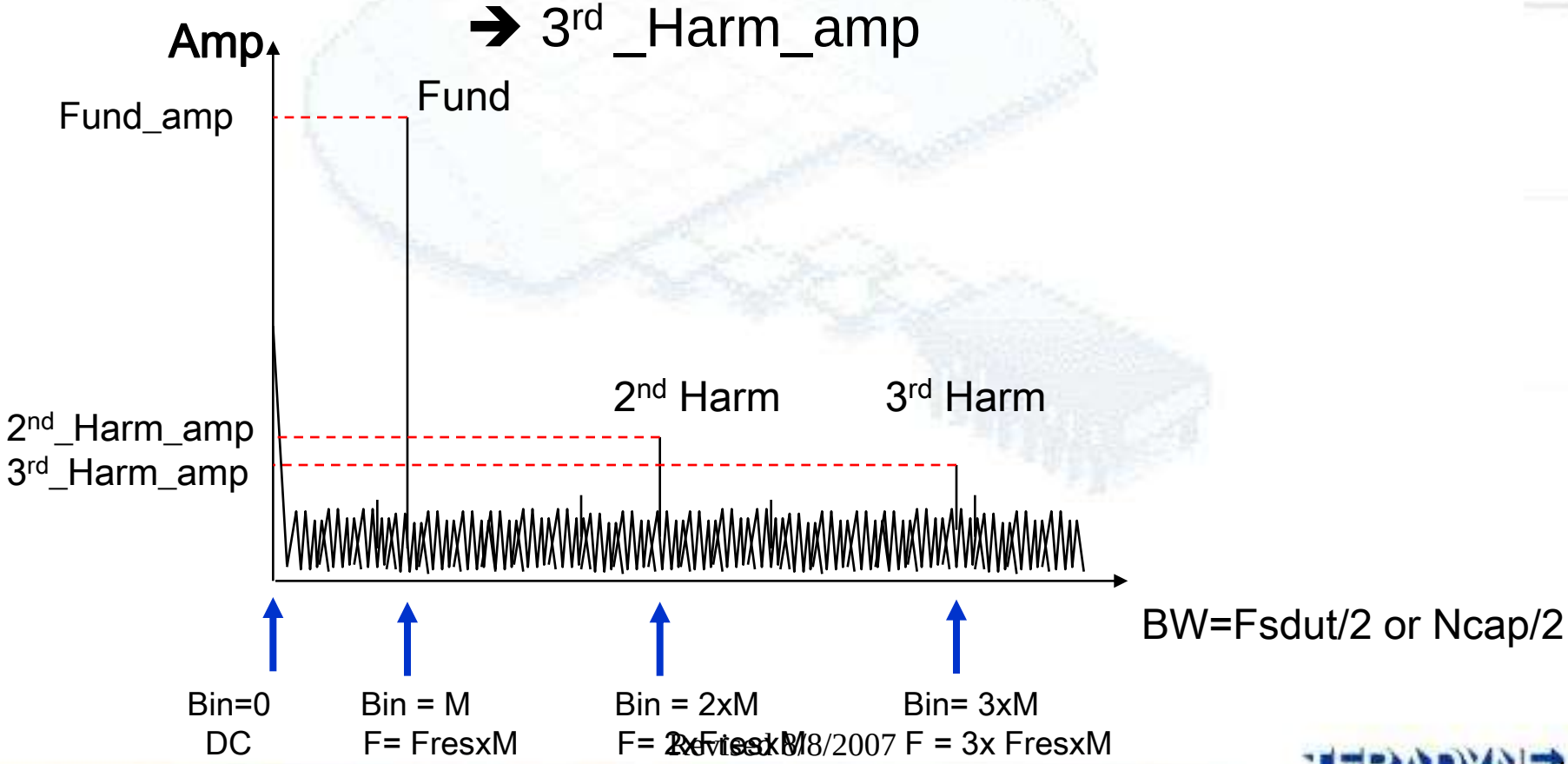


DAC DYNAMIC TEST METHODOLOGY

SNR, THD, SINAD tests:

Step 2. Store 2nd and 3rd Harmonic amplitudes:

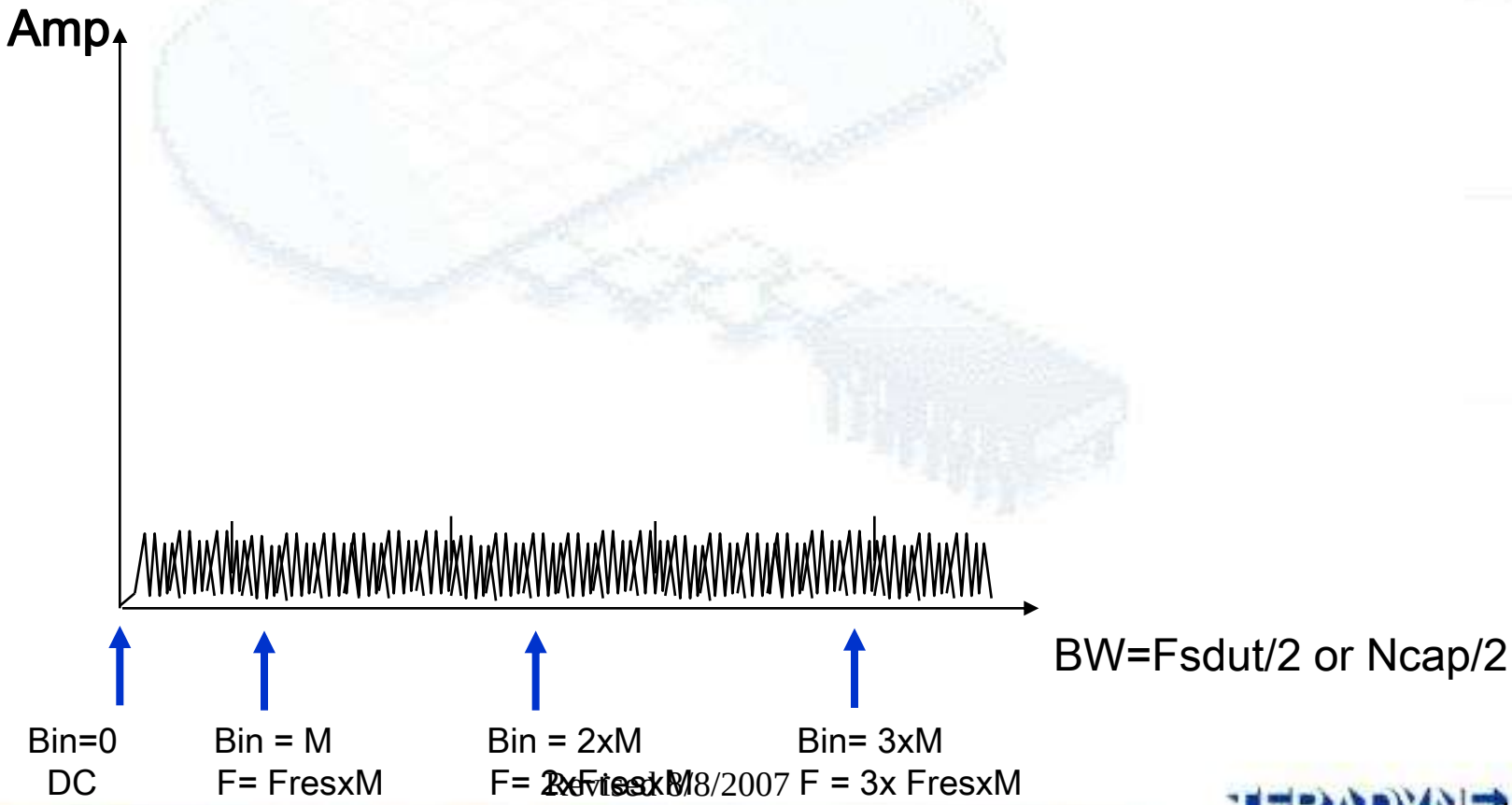
- ➔ 2nd_Harm_amp
- ➔ 3rd _Harm_amp



DAC DYNAMIC TEST METHODOLOGY

SNR, THD, SINAD tests:

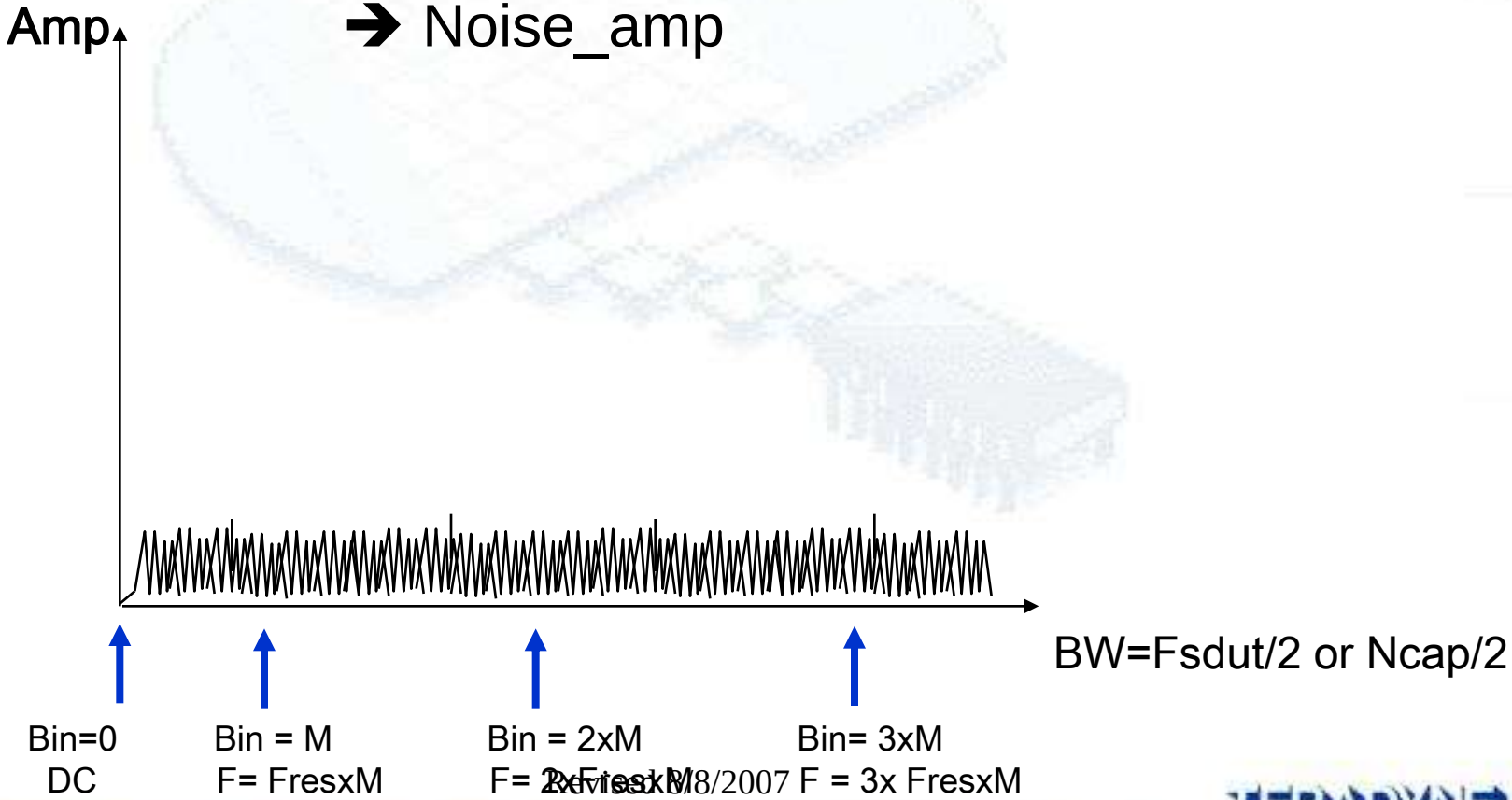
Step 3. Zero out the DC, Fund and Harmonics:



DAC DYNAMIC TEST METHODOLOGY

SNR, THD, SINAD tests:

Step 4. Sum all remaining Bins.
Store results as Noise
➔ Noise_amp



DAC DYNAMIC TEST METHODOLOGY

SNR, THD, SINAD tests:
Step 5. Compute results

Signal-to-Noise Ratio (in dB)

$$= 10\log [(\text{Fund\_amp})/(\text{Noise\_amp})]$$

Total Harmonic Distortion (in dB)

$$= 10\log[(2^{nd}\text{\_Harm\_amp} + 3^{rd}\text{\_Harm\_amp})/(\text{Fund\_amp})]$$

Signal-to- Noise+Distortion (in dB)

$$= 10\log[(2^{nd}\text{\_Harm\_amp} + 3^{rd}\text{\_Harm\_amp} + \text{Noise\_amp})/(\text{Fund\_amp})]$$

Self-Assess Questions

What does the below parameters stand for:

FSR, INL, DNL, SINAD

What is the input signal (DC, ramp, sinewave etc) used for testing

ADC, DAC

Which needs to have lower Noise Floor?

Digitizer or DUT (for DAC test)

AC source or DUT (for ADC test)

You have a 11-bit AC Src. This instrument should be suitable to generate an input signal to test which of the below?

8-bit ADC, 11-bit ADC, 8-bit DAC, 14-bit DAC

DEBUG TOOLS AND DEBUGGING

TERADYNE

Debugging Tools

Basic Tester Debugging Tools are:

- Datalog
- Histograms
- Characterization : - Shmoo , Margin
- Pattern Debug
- Waveform

Debugging Tools

DataLog

- Provides information on what tests are passing and what tests are failing
- Helpful in determining if failure is gross or marginal
  - Gross: Failed multiple or successive tests
  - Marginal: Failed one or few tests with reading close the limit

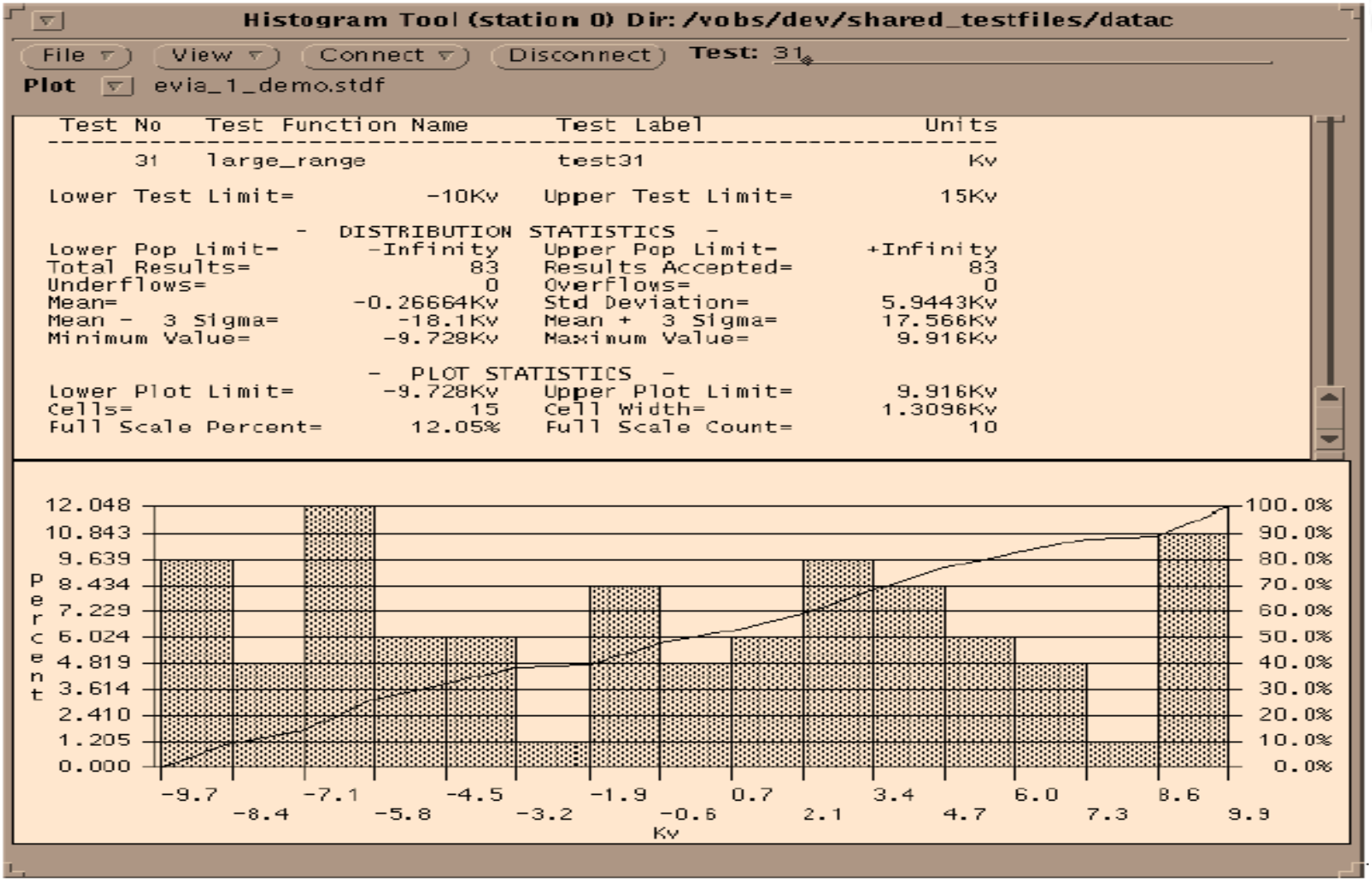
Debugging Tools

Histogram

Provides:

- Distribution of results/readings for specific test
- Information on how much yield recovery can be achieved when the limit is changed
  - Derive optimum limit adjustment to maximize yield
- Information of rejects test results with respect to limits.

Histogram Plot



Revised 8/8/2007

Characterization

- The purpose of characterizing a device is to determine the extremes at which the device will still be operational.
- It involves experimenting with the DUT (different operating environment) to investigate its behavior using varying input conditions.
- Certain combinations of input parameters can cause the DUT to pass/fail. Analyzing these pass/fail regions can tell a lot about the manufacturing process and the suitability of the chosen test limits.
- Characterization can be performed as part of the regular testing process, or interactively while trapped at a breakpoint.

Characterization Tools

The following Characterization Tools are commonly used:

- **Shmoo**
  - 1-Dimensional Shmoo (X-axis only)

    Vary one parameter or spec over a range while recording Pass/Fail/Error results and if the tests provides, the measured value for each point
  - 2-Dimensional Shmoo (X and Y-axis)

    Vary 2 parameters or specs over a specified ranges
  - 3-Dimensional Shmoo (X, Y and Z-axis)

    Vary 3 parameters or specs over a specified ranges
- **Margin**

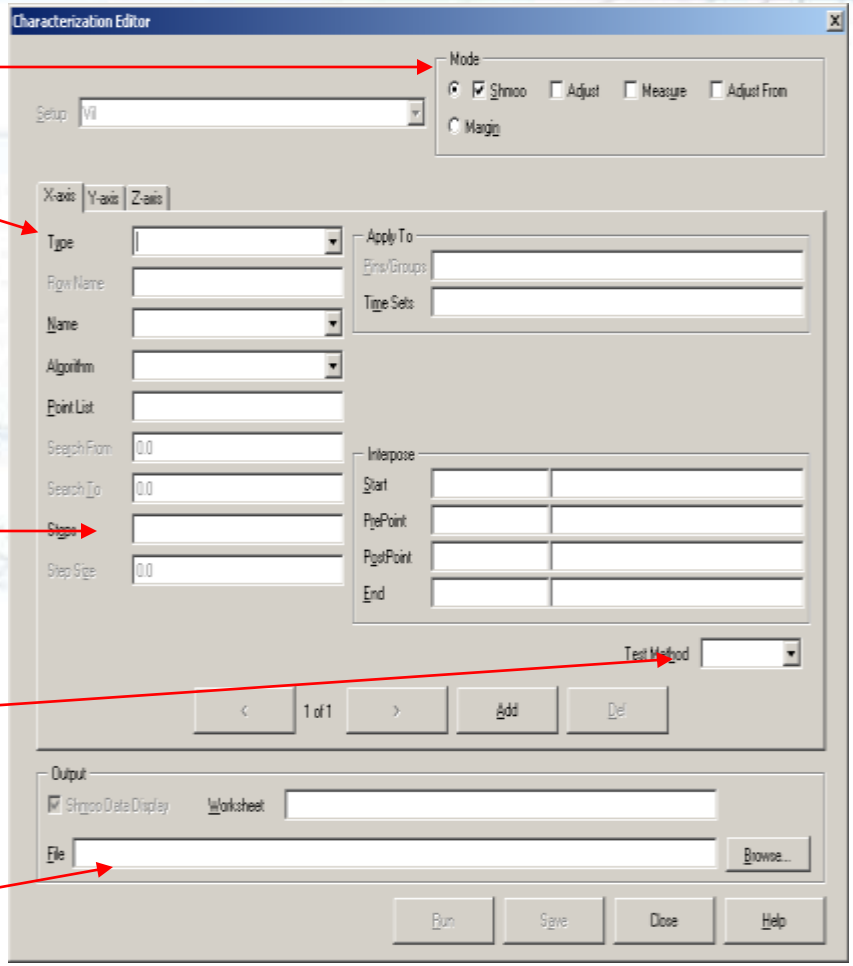
  Vary one parameter or spec over a range. Similar to 1- Dimensional Shmoo.

Generating Characterization Data

- The following steps are used to setup and execute a Characterization Event:
  1. For each Characterization Event ,
     - Create Setup
       - Name
       - Mode
       - Parameters to Vary
       - Range
       - Point Generation
  2. Execute the Characterization Setup either
     - from Test Flow
     - Interactively

Characterization Editor Entries

- **Mode Selection**
- **Type of Parameter to Vary**
  - Spec (AC Spec, DC Spec)
  - Level
  - Edge
  - Period
- **Search Range**
  - Search From
  - Search To
- **Test Method**
  - Retest (execute instance)
  - Reburst (execute pattern burst)
- **Output Selection**
  - Worksheet
  - File



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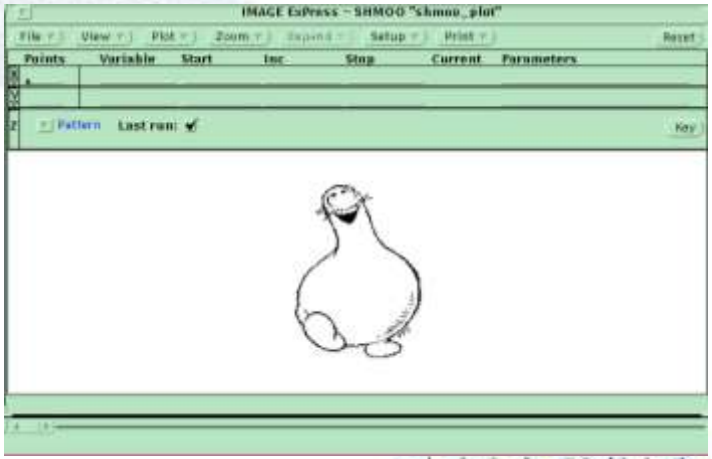
Shmoo

Shmoo

- Shmoo is a utility to debug and characterize devices.
- Shmoo is useful for determining the passing limits of voltage, current, timing or other device parameters while fine tuning the test program for its specific application.
- Shmoo produces a graphical plot or view of the behavior of a device under test (DUT) while the value (settings) of control parameters are changed.



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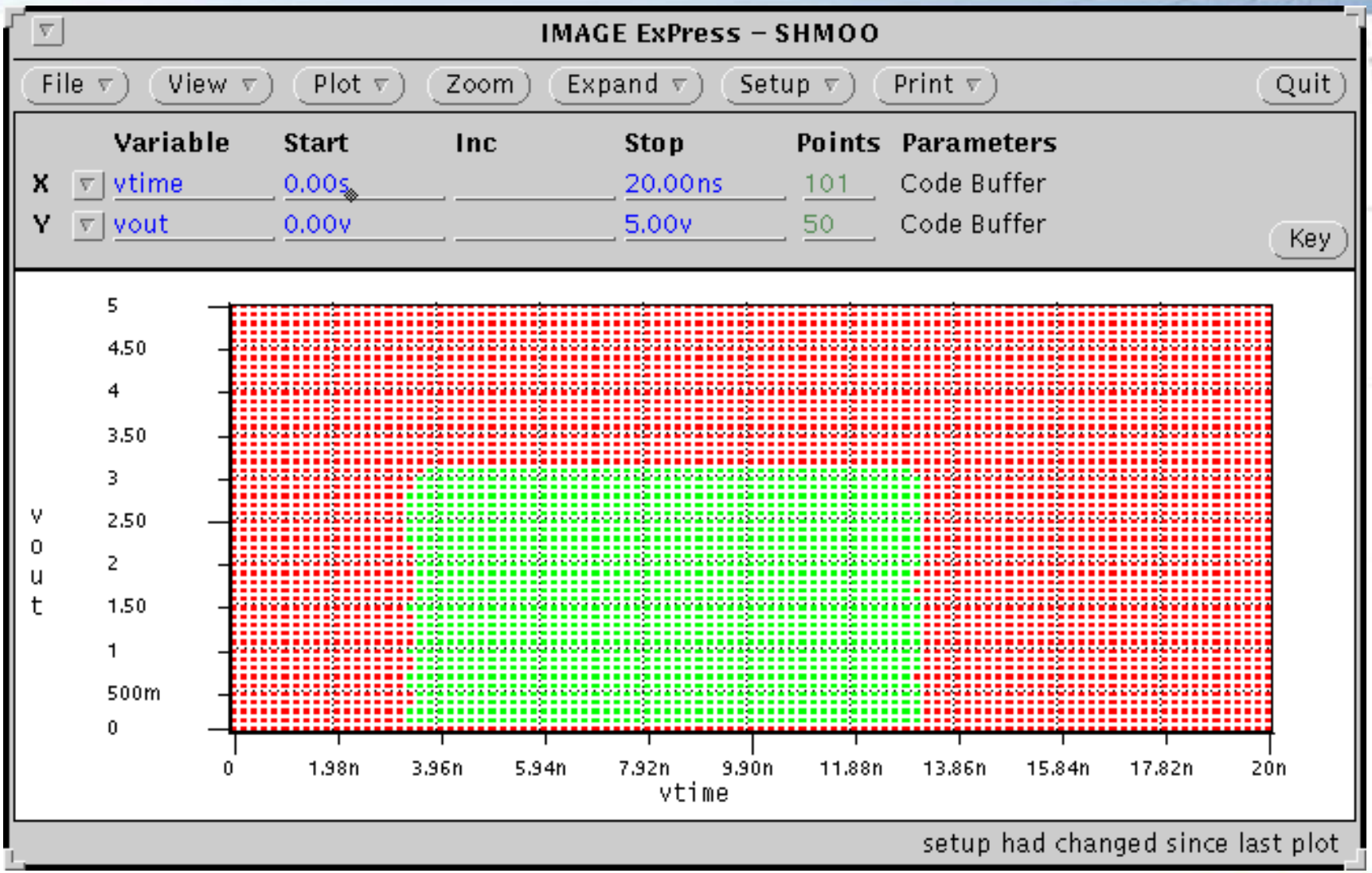
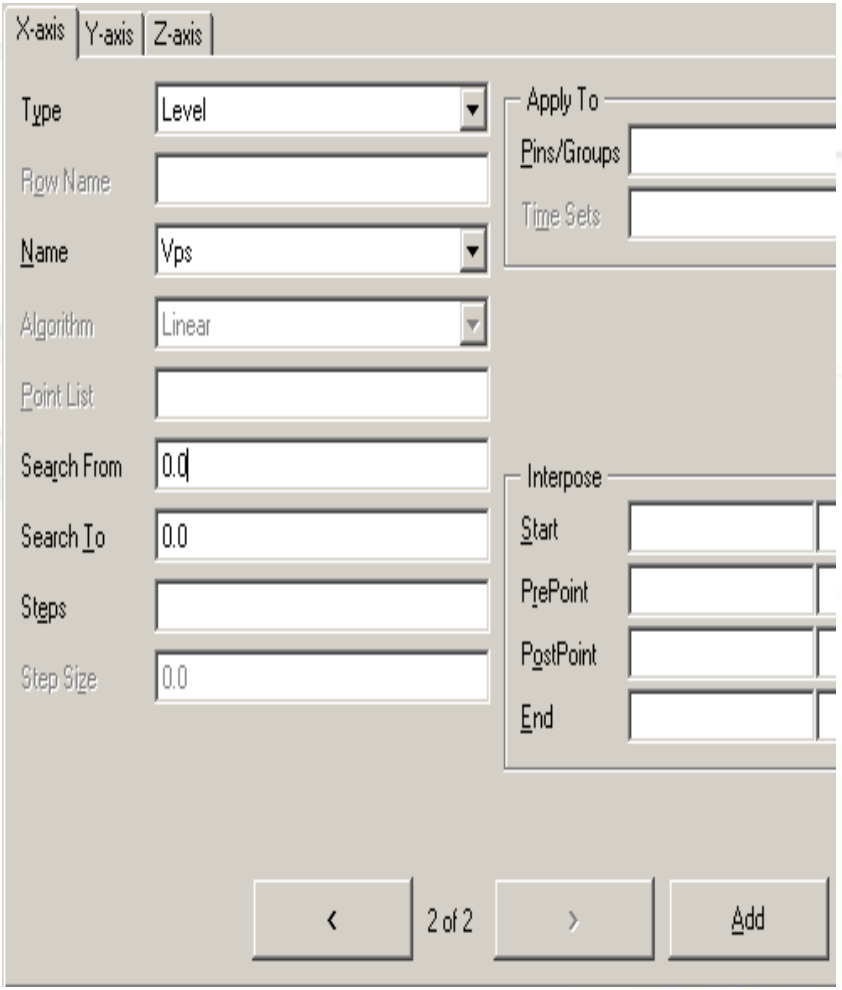
Shmoo Result



Shmoo Setup - Tracking Parameters

- A Shmoo Plot can allow multiple parameters to be varied along an axis.
- The first parameter is generally defined for an axis as the *'Primary'* parameter. All other parameters for that axis are *'Tracking'* parameters.
- A Tracking parameter will always use a Linear Search Algorithm. Each Tracking parameter will have its own range but will change in *'lock step'* with the Primary parameter.



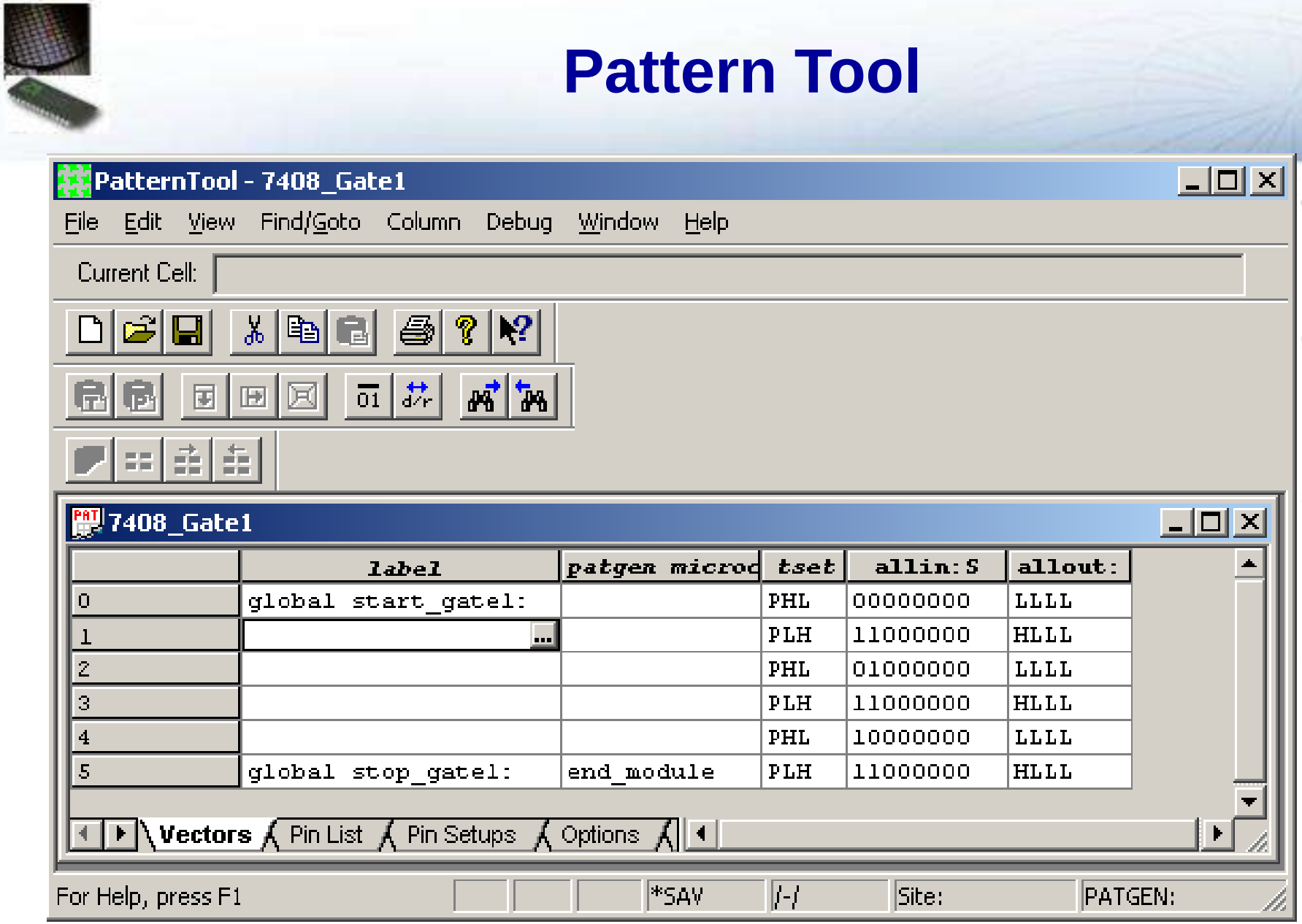
Debugging Tools

Pattern Debug

- History Ram (HRAM) provides information on Pass/Fail vector (first failing vector, failing vector count etc) and device pin information (which pin fail, how many pins fail etc).

- Logic Analyzer provides information on expected logic state as well as actual device pin state with respect to voltage levels / timing edges.

Pattern Tool



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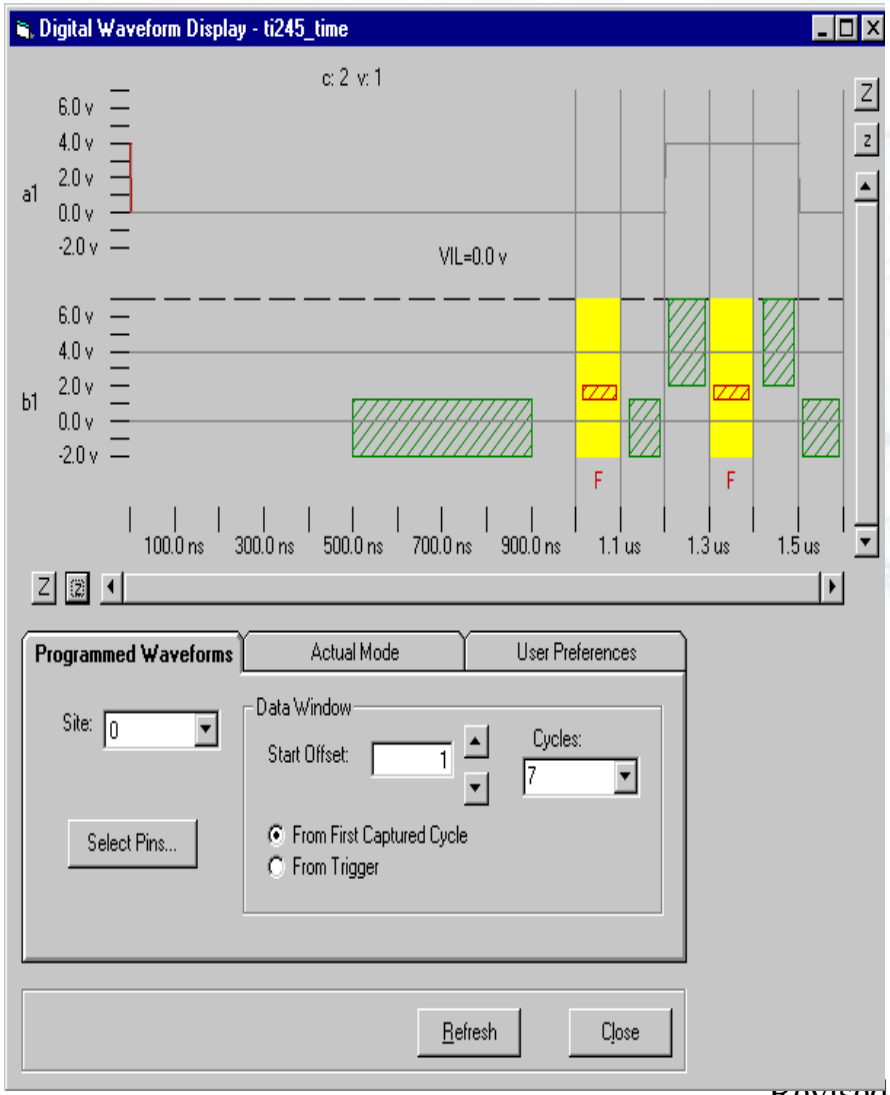
Debugging Tools

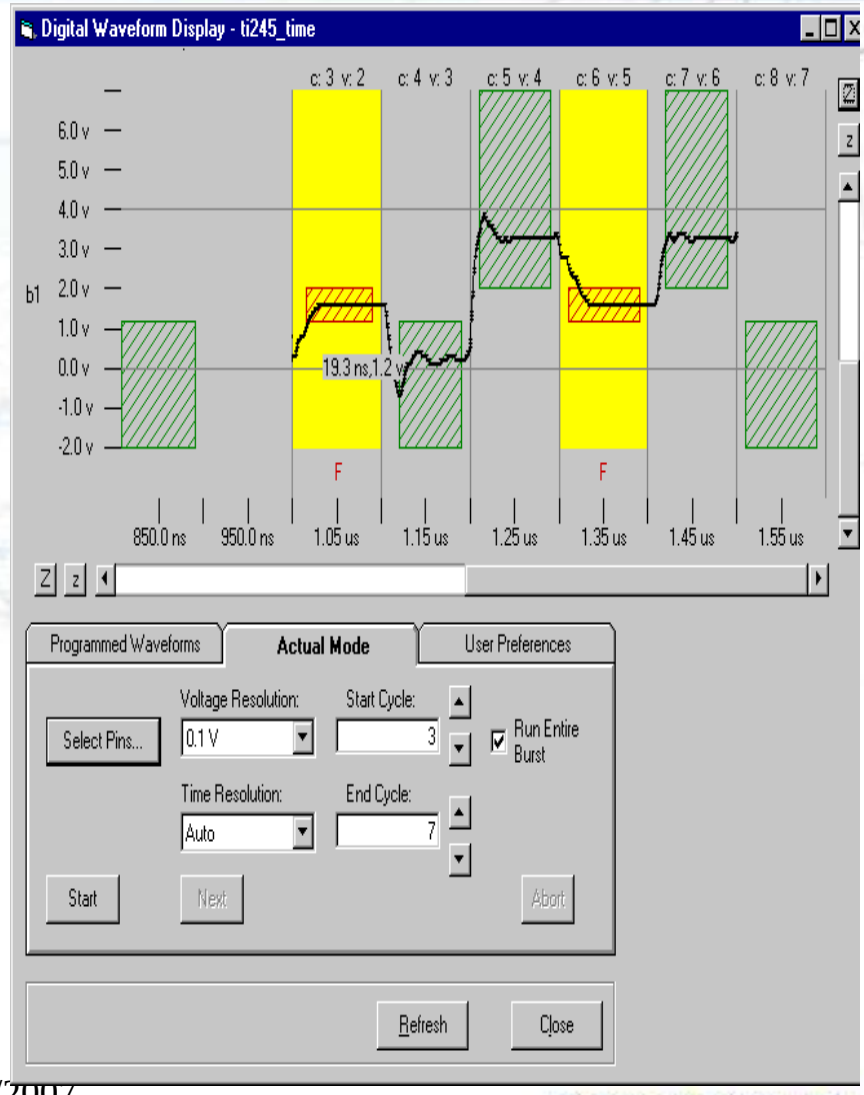
Waveform Tool

- The waveform tool is a very useful tool for debugging, especially in analog/mixed-signal tests

- Display actual waveform of input and output signals, amplitude, timing, frequency information.

Waveform Tool





Possible Cause for a Failure

The possible cause for a test failure could be any of these

- DUT failure
- Test hardware interface problem
  (Loadboard, socket, pogo pins)
- Test system
- Test program

Trouble-shooting is needed to identify the exact cause of the failure

Basic Troubleshooting Techniques

- Run the test and get the Test Datalog.
- Finding out what is failing from Datalog.
- Check if Failure Continuity, DC, Functional or Leakage

The following slides will explain “what to check?” and the “Purpose of these checks”

Basic Troubleshooting Techniques

Continuity Failure

What to Check

1. Identify failing pin from datalog.

2. Check the failure pin reading.
   Trace circuit path along the connection (Testhead up to DUT pin) using an external meter.

3. Verify if a problematic contact is at receptacle, socket or DUT itself.

Purpose

- Isolate failing DUT pin
- Check for open or short failure.
- Identify specific area of problem (Testhead, loadboard, receptacle, socket, DUT pin)

Basic Troubleshooting Techniques

What to Check	Purpose
4. Verify Loadboard for any wire disconnected.	• identify wiring/loadboard problem
5. Test a known good device.	• isolate if it is a device problem.
6. Restart and recalibrate the tester (if known-good device also fails)	• Check if it is a test system problem

Basic Troubleshooting Techniques

Leakage Failure

What to Check

1. Identify failing pin from datalog
2. If marginal:
   - Try adding/increasing settling time prior to meter measurement.
   - Try relaxing input level (VIL/VIH) prior to pattern run.
   - Recommend for limit relaxation.
3. If gross failure:
   - Verify if precondition pattern is passing.
   - Try adjusting input or output timing.

Purpose

- Determine whether the failure is gross or marginal.
- Recommend probable fix for gross and marginal failures.

Basic Troubleshooting Techniques

Digital Functional Failure

What to Check

1. Identify VDD level failure using datalog (Continue-on-fail).
2. If marginal, check ‘ringing’ at supply, check filter capacitors.
3. Do functional debug using tools like Pattern Debug, Logic Analyzer and Shmoo plot.
4. Adjust timing/levels/mask transition points whichever is applicable based from item 3 analysis.

Purpose

- Determine failure is at which VDD level (min, max or nom), check for marginality.
- Ensure that filter capacitors are in place and good.
- Determine if it is timing/levels related. Check critical transition points.
- Check criticality of input levels.
- Determine impact of Program change if the problem can be resolved.

Basic Troubleshooting Techniques

Other Functional Failure

What to Check

1. Identify failing DUT pin and test.
2. Check if precondition pattern fails using digital debug tools.
3. Using waveform tool, check waveform at Input and Output.
4. Using a scope, trace signal from input to output at different points along the path.

Purpose

- Determine specific test and DUT pins failing.
- Determine whether failure is caused by pattern.
- Determine if tester is supplying, and capturing the expected signals
- Determine at which point along the path, the signal is degrading or missing.

Production-Ready Test Program

- Customer's Approval
- Repeatability check
- Test Program Backup
- Test Plan Matrix
- Loadboard Schematic
- Test Program Revision Number, Date and History
- Full Datalog for 10 Good units

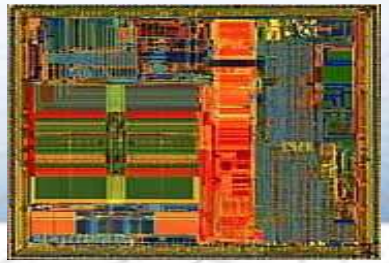
Self-Assess Questions

- What is the purpose of doing device characterization?
- What is the different between Shmoo and Margin Tool?
- State 3 possible causes of a test failure

INTRODUCTION TO DESIGN-FOR-TESTABILITY (DFT)

TERADYNE

Design For Test or DFT



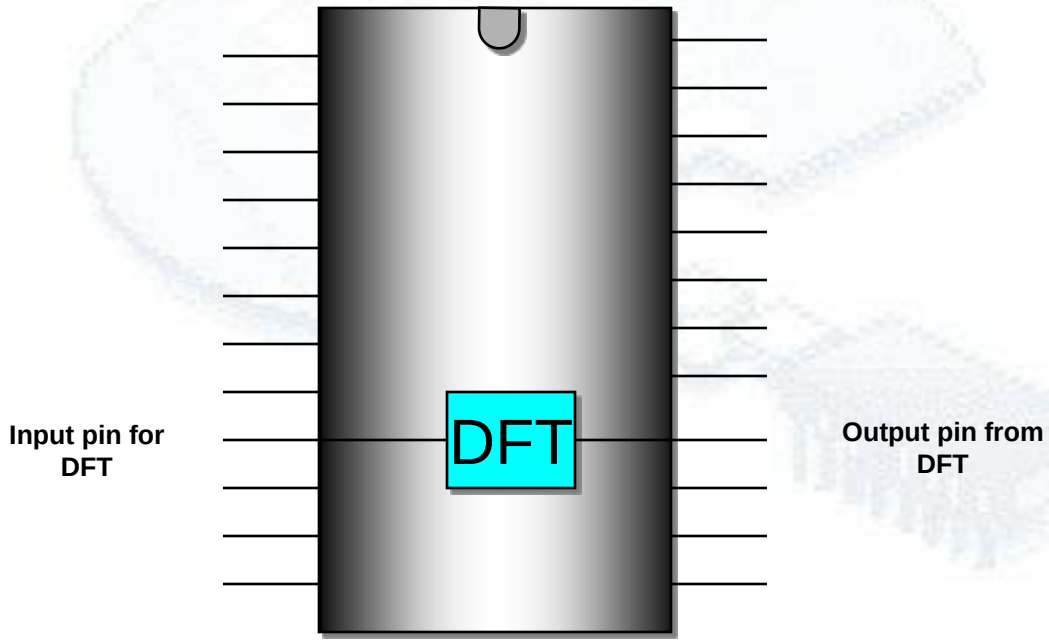
- Delay-inducing defects are causing increasing concern in the semiconductor industry today, particularly at the leading-edge 130nm and 90nm nodes. To effectively test for such defects, the at-speed behavior of the logic has to be emulated in the most cost-effective way possible.

- Design for test is the test concept with which ,while designing a chip, a small module is added to test its functionality.

- DFT refers the design technique that make test generation and test application cost effective.

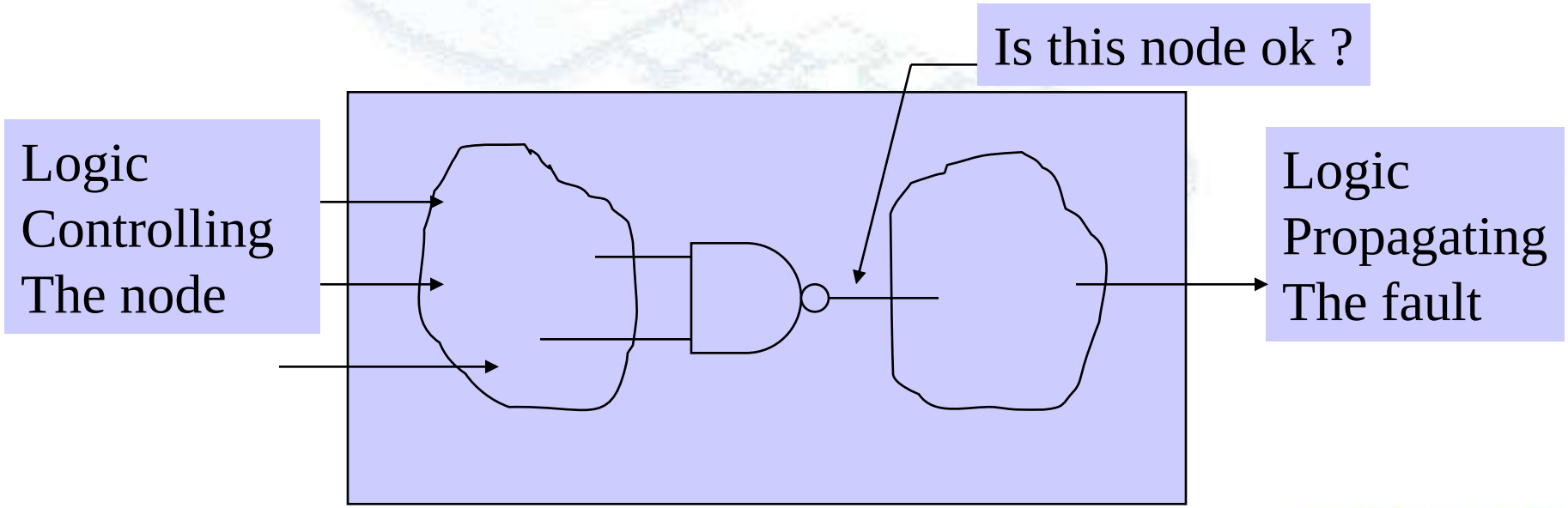
Design For Test

Chip with DFT Module



Testability - DFT

- An internal fault can be very difficult to check if there is no specific structure.
- It can only be tested if the input of the structure can be controlled and the output can be observed.
- An ideal case would require that all nodes can be controlled and observed.



Why Design For Test

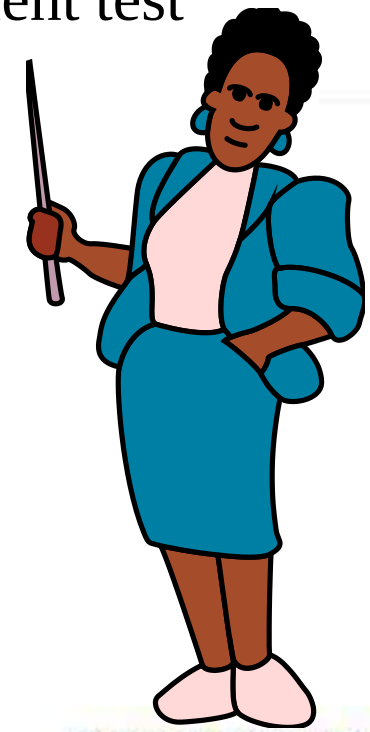
- High speed testers are very costly
- Reducing test time can help increase throughput of tester, this impacts (lowers) testing cost
- Testing must be considered at early phases of the design process

Cost of Testing

- Design for testability (DFT)
  - Chip area overhead
  - Performance overhead
- Software processes of test
  - Test generation and fault simulation
  - Test programming and debugging
- Manufacturing test
  - Automatic test equipment (ATE) capital cost
  - Test center operational cost

Advantages of DFT

- Directly observable internal nodes.
- Direct controllability of internal nodes.
- Enables combinational ATPG.
- Multiple balanced scan chain results in very efficient test vectors.
- Efficient diagnostic capability.
- Enables testing of both timing and structure.



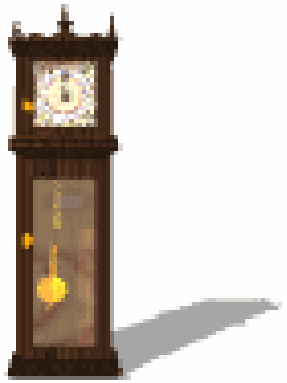
Disadvantages of DFT

- Scan hardware increases chip size.
- Compressed scan vectors increases the chips power consumption.
- Design rules may require bypass clock inputs.
- May have a large impact on total design budget.
- Requires additional control logic to guarantee safe scan shifting and sampling.
- Requires more concern about clock-delay and clock-skew.

Benefits and Trade-offs of DFT

The major benefits of using Design for Testability are:

- Shorter time to market
- Reduced test time
- Inexpensive test equipment
- Yield learning, which is often overlooked



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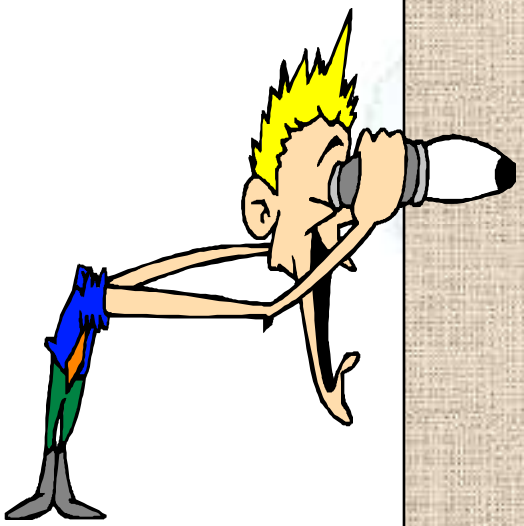
Benefits and Trade-offs of DFT

The implementation of DFT involves some sacrifices

- Increased area of components
- More pins on the PCB
- Increased PCB area

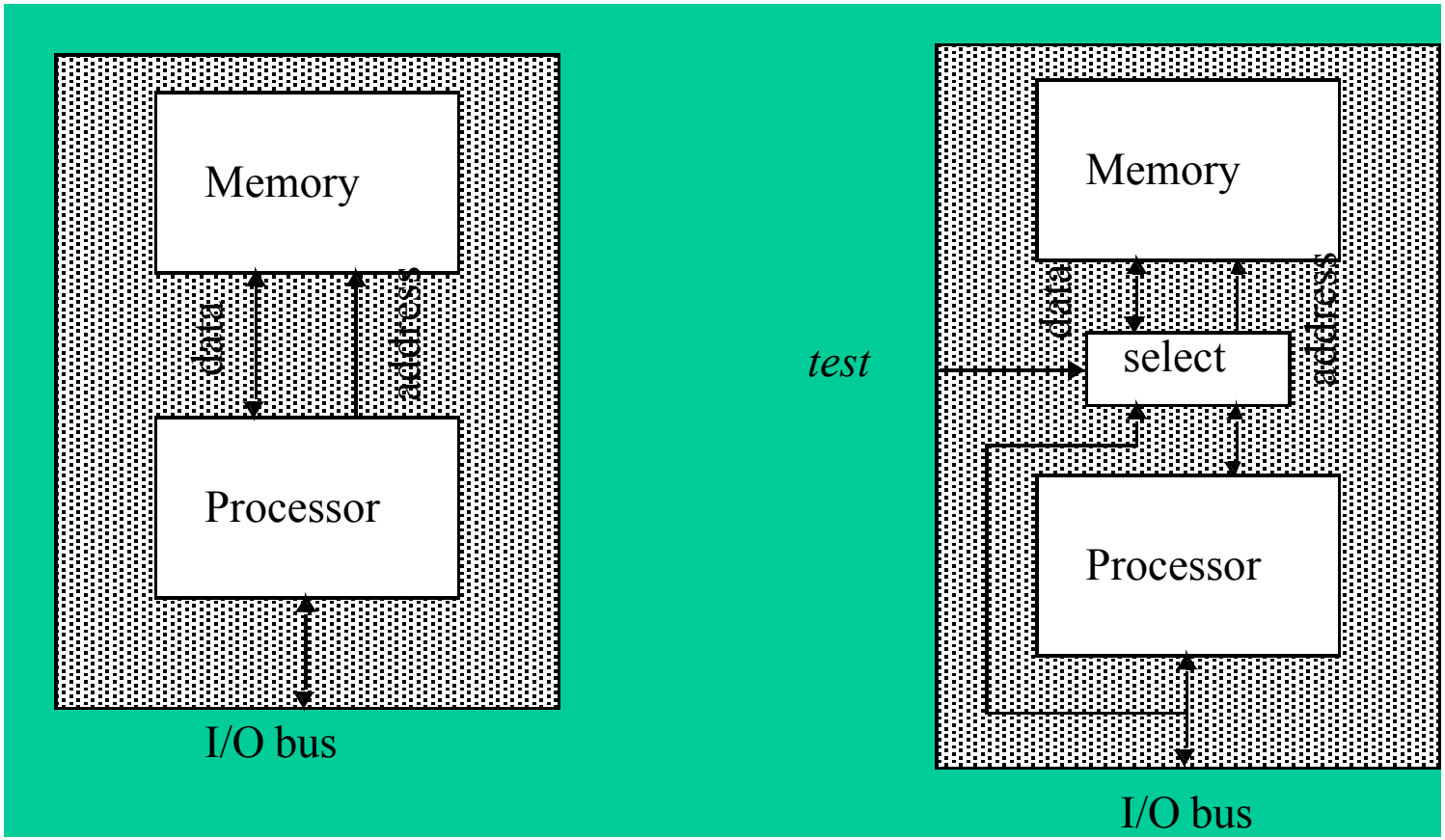
Test Approaches



Three approaches

- Ad-hoc testing
- Scan-based testing
- Self-test

Ad-hoc Test



Inserting multiplexer improves testability

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Ad-hoc Test

For Ad-hoc test ,Good design practices learnt through experience are used as guide lines

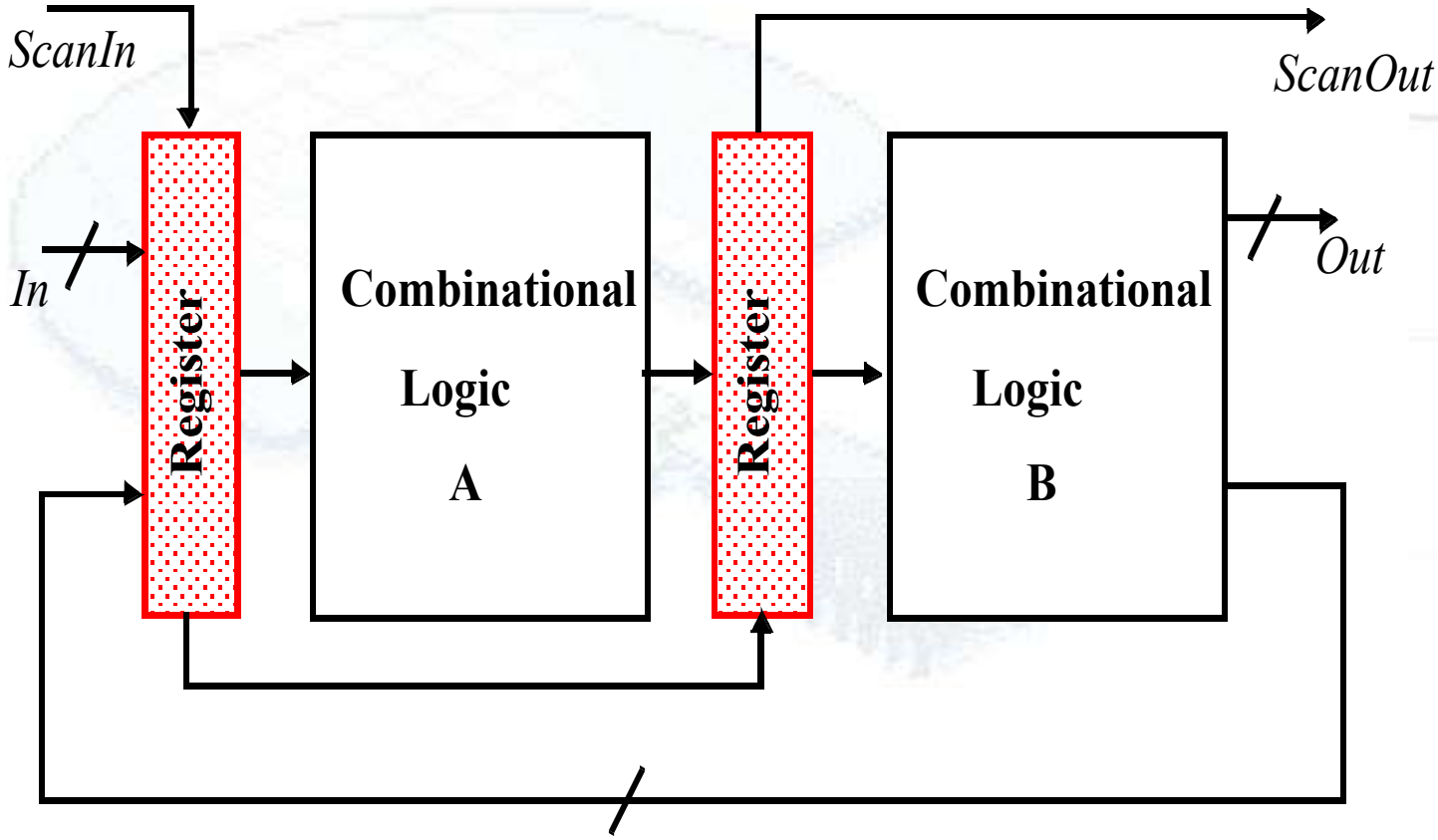
- Avoid Asynchronous (un-clocked) feedback
- Make flip-flop initialize
- Avoid redundant gates. Avoid large fan-in gates
- Avoid gated clocks
- Design reviews conducted by experts or design auditing tools.

Disadvantages of Adhoc testing

- Experts and tools not always available
- Test generation is often manual with no guarantee of high fault coverage
- Difficult to estimate/guarantee fault coverage
- Design iterations may be necessary

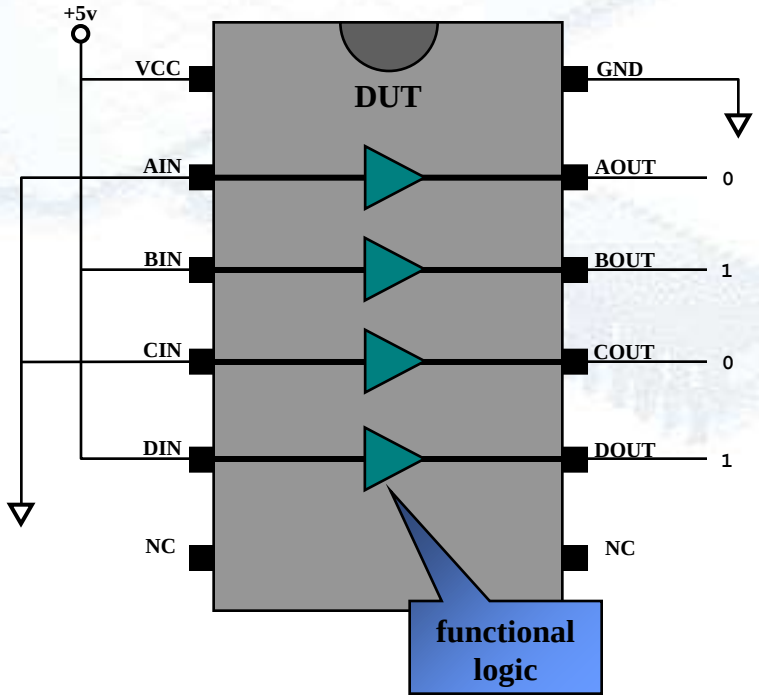
These techniques can be used for small designs

Scan-based Test



Introduction to Scan

- A typical device, without scan cells, processes data through the functional logic as usual.



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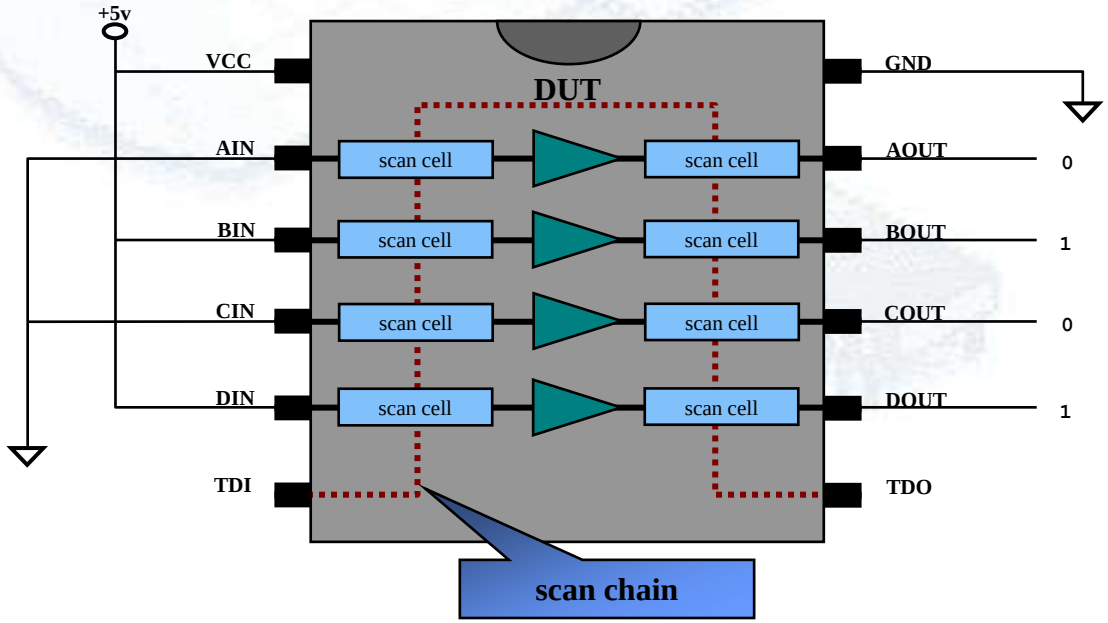
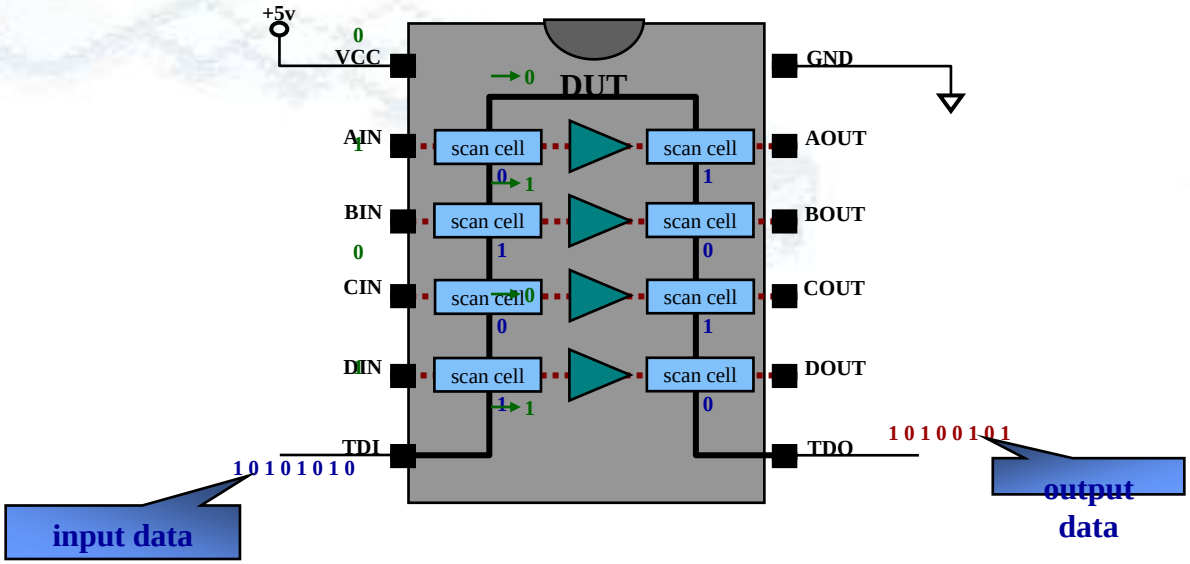
Scan Cells

- Likewise, device with scan cells can process data through the functional logic as usual, bypassing the scan chain.
- Here, data passes between device pins and the functional logic through scan cells.



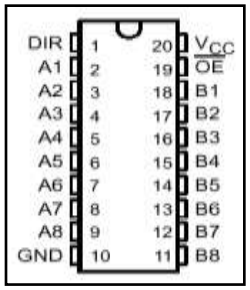
Scan Chain

- However, a device with scan also allows data to be loaded through the scan chain and stored in the scan cells.
- The data is then processed through the functional logic, changing the values stored in the output scan chains.
- The output scan data can then be checked by shifting the data out the scan chain.

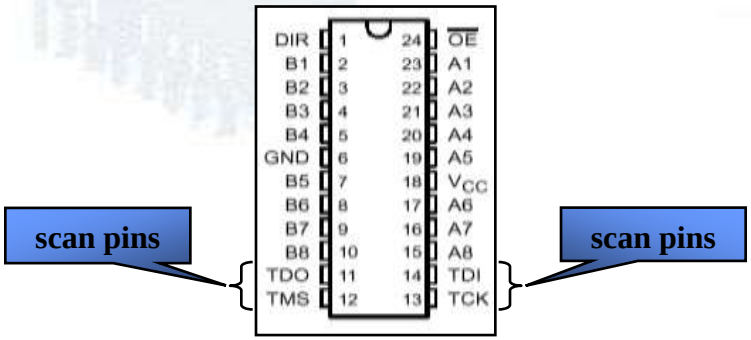


Microcircuit Testing

- Device designer develops scan vectors automatically using fault coverage and test simulation tools.
- Scan reduces test program development time.
- Scan allows direct access to the device registers reducing test time by removing unnecessary overhead though functional test methods.
- Scan improves fault coverage and diagnostics at device and board test.



SN74BCT245
octal bus transceiver



SN74BCT8245A
octal bus transceiver with scan

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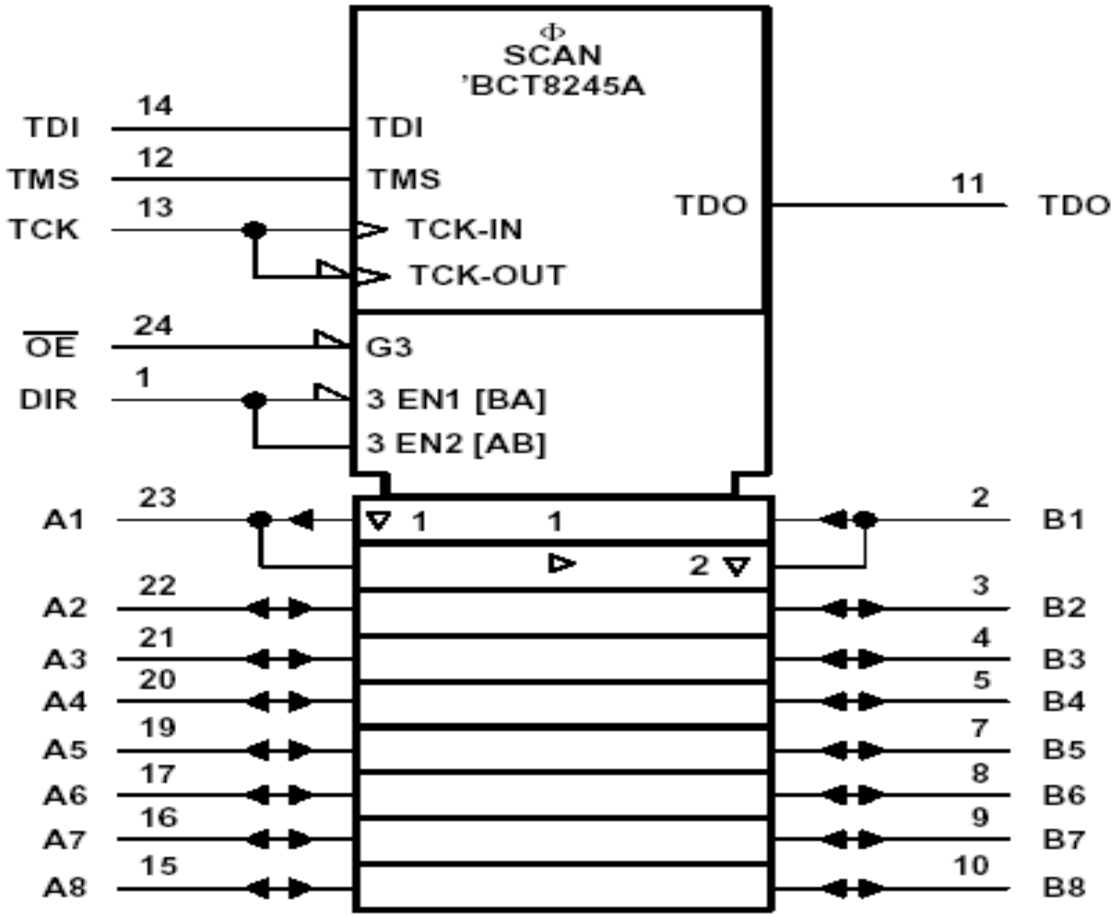
SN74BCT8245A With Scan



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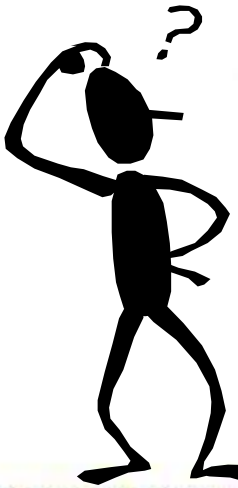
Why Scan Test

- In a sequential circuit it is difficult to form test vectors for stuck-at-faults because the sequential depth of the design easily makes the test vectors to large.

- The main idea with scan design is to obtain control and observe flip-flops and thus making it easier to form test vectors.



Scan Design

Circuit is designed using pre-specified design rules.
Test structure (hardware) is added to the verified design.

- Replace flip flops by scan flip flops (SFF) and connect to form one or more shift registers in the test mode

- Make input/output of each scan shift register controllable or observable from PI/PO

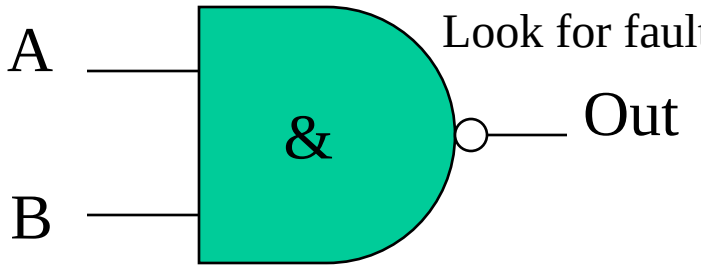
- Use ATPG tools to obtain tests for all testable faults in the combinational logic

- Add shift register tests and convert ATPG tests into scan sequences for use in manufacturing test

A fault model : Stuck @ 0/1

- The fault model is commonly used for Logic device
- It is applied on primitive elements such as Nand/Nor gates…
- The model can be extended to Nodes
  - Stuck at zero or node stuck at logic 0
  - Stuck at one or node stuck at logic 1

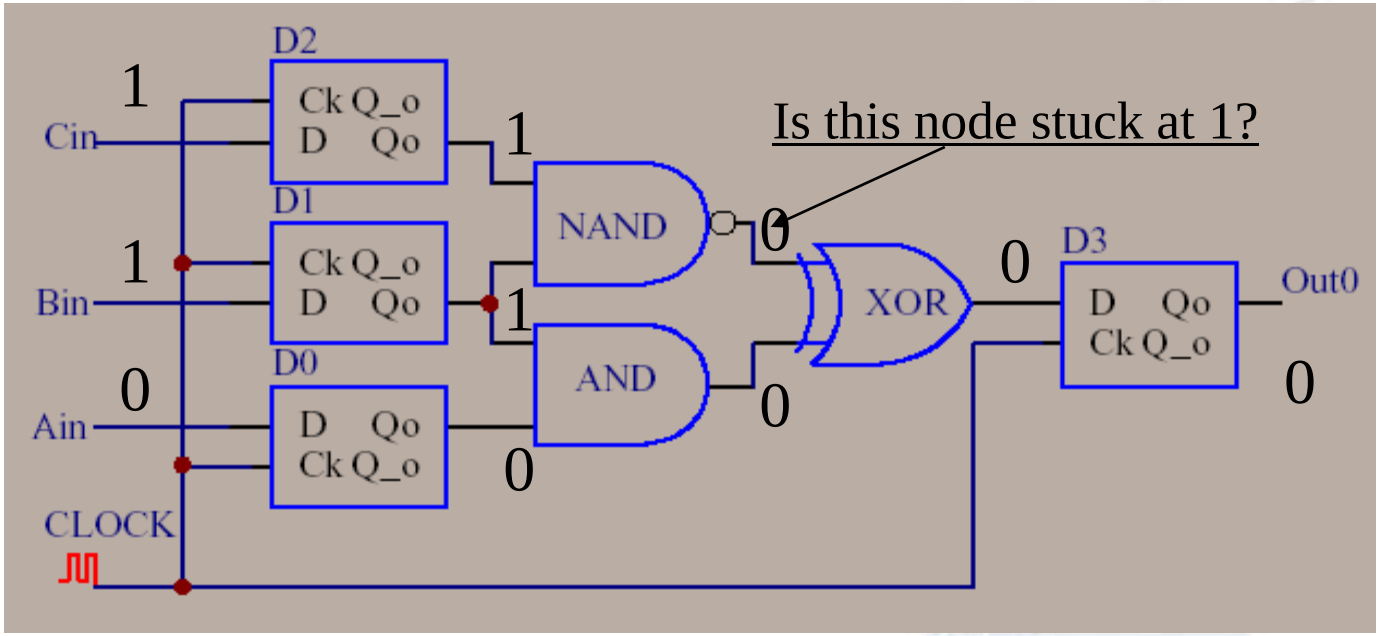
Set input condition



Look for faulty output

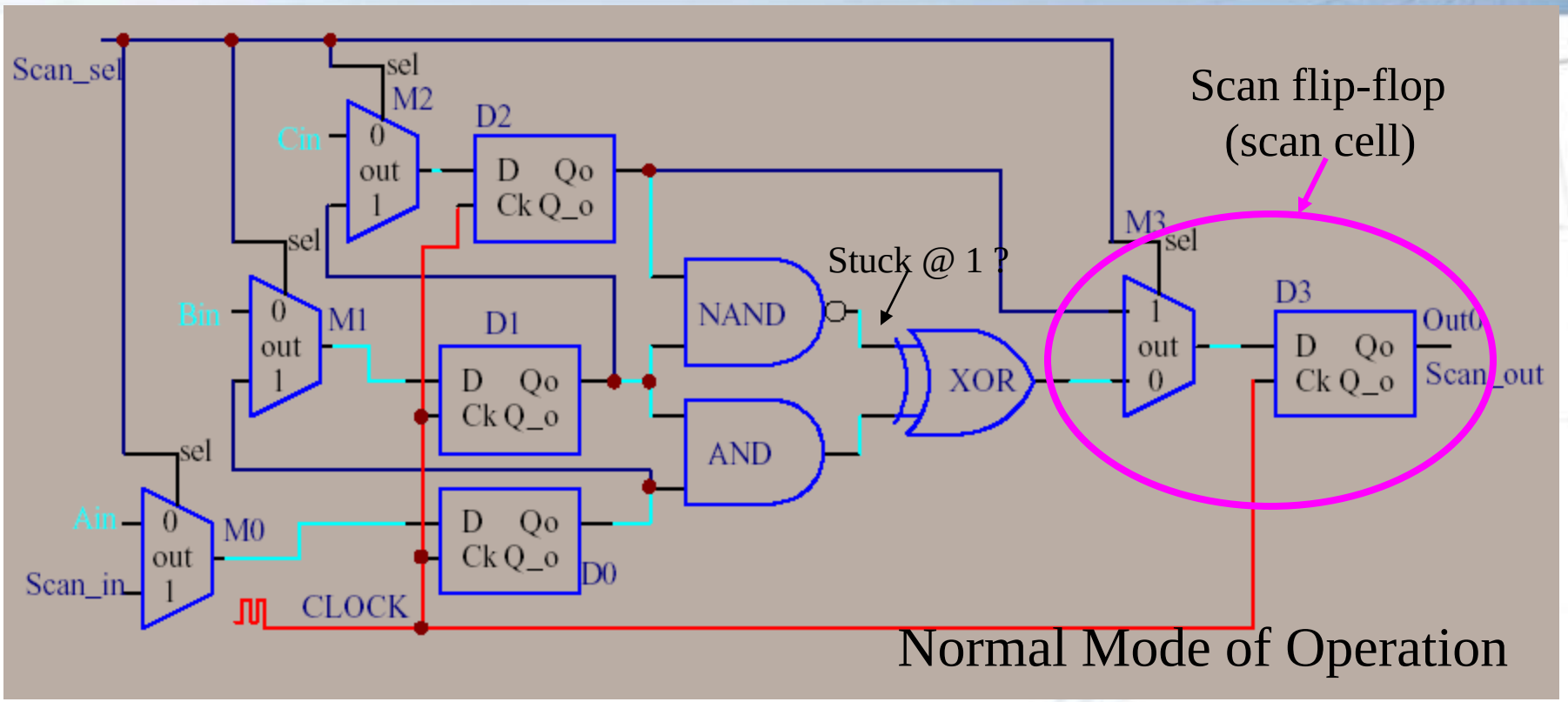
A	B	Out	FAULT
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

Design Example



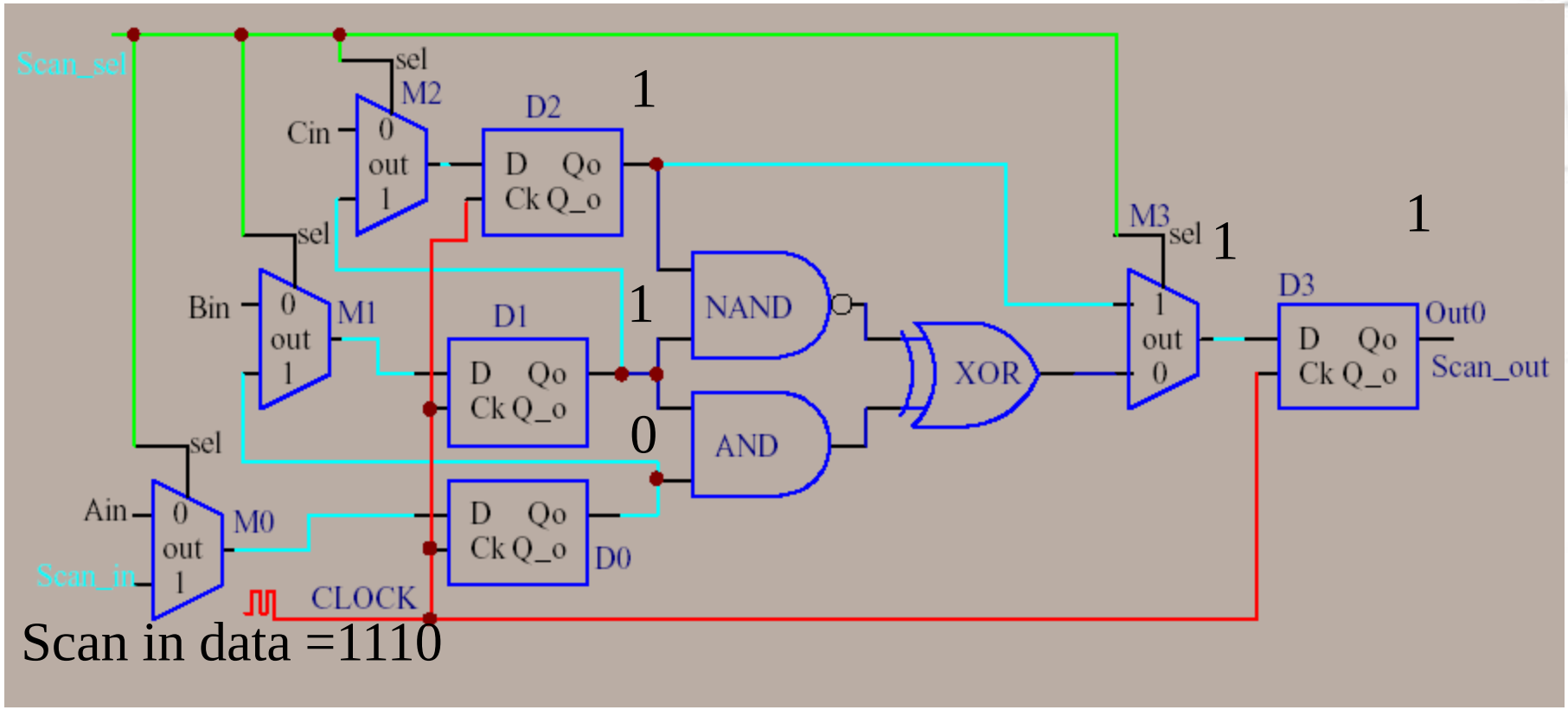
- To check the node, Ain, Bin and Cin should be at the following values 0,1,1. If it is stuck at 1, the fault propagates to OUT0.
- How to do that if the inputs are not easily accessible ?

Design Example (cont..)



- Add a multiplexer to every flip-flops, chain them together
- Add a Scan_sel signal to select the mode and a Scan_in to provide data

Design Example (cont..)

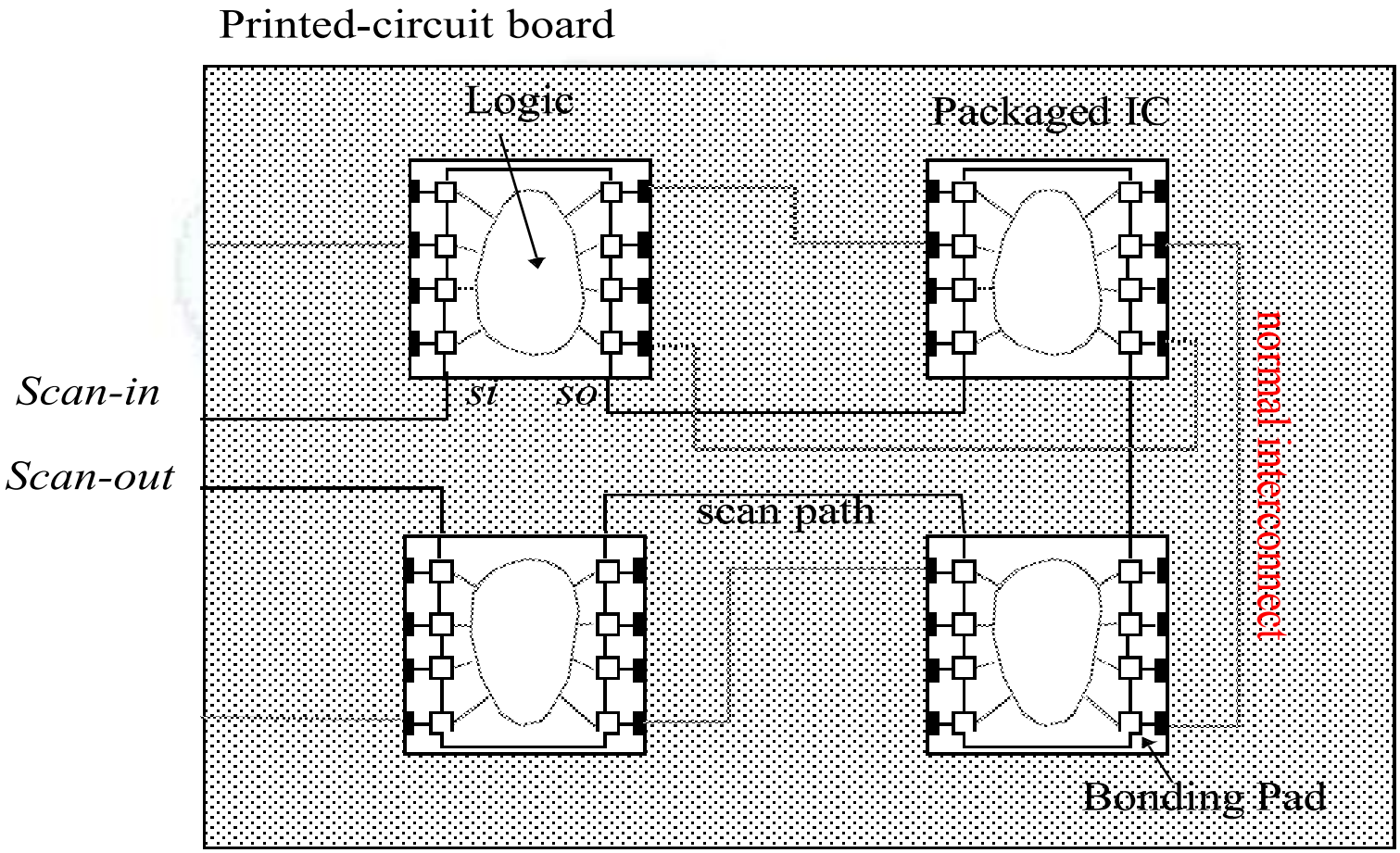


- Select the scan mode and scan data in. (4 clocks needed)

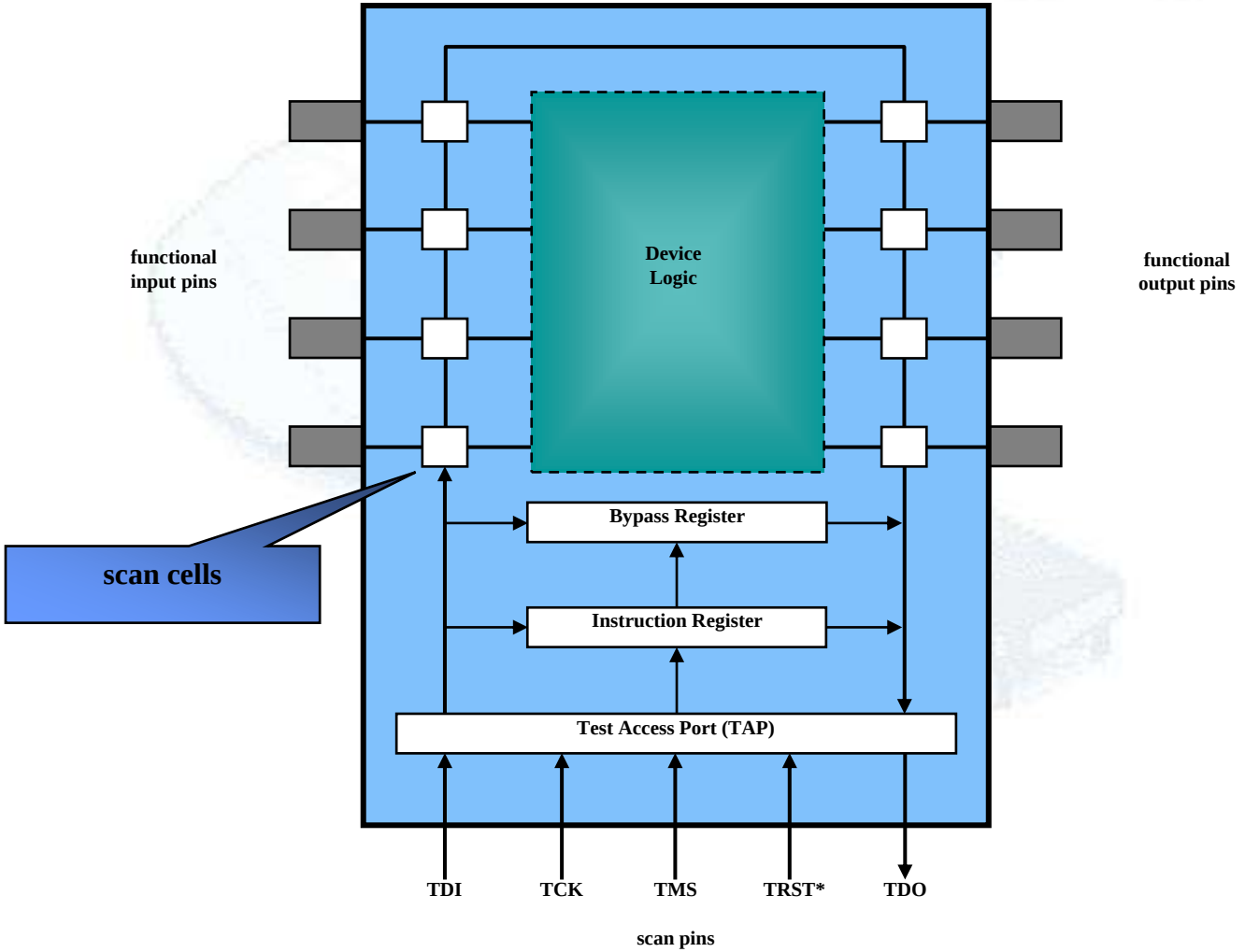
More about Scan

- Scan is the most popular DFT technique
  - Rule based design
  - Automated DFT hardware insertion
  - Combinational ATPG
- Advantages
  - Design automation
  - High fault coverage;helpful in diagnosis
  - Hierarchical-scan testable modules are easily combined into large scan-testable systems
  - Moderate area (~10%) and speed (~5%) overheads
- Disadvantages
  - Large test data volume and long test time
  - Basically a slow speed(DC) test

Boundary Scan



Boundary-Scan Architecture



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Boundary-Scan

- Boundary-scan testing is controlled by a Test Access Port (TAP) Controller.

- The TMS, TRST, and TCK pins operate the TAP controller, and the TDI and TDO pins provide the serial path for the data registers. The TDI pin also provides data to the instruction register, which then generates control logic for the data registers.

Scan Standard

- The IEEE Std. 1149.1 was approved by the Joint Test Action Group (JTAG) on February 19, 1990.
- As a result, IEEE Std. 1149.1 is often referred to as JTAG 1149.1 boundary scan.
- The scan interface uses a block of control logic called a *test access port* (TAP).

Scan Standard

- Scan architecture uses five signals;
  1. Test Clock (TCK)
  2. Test mode select (TMS)
  3. Test Data in (TDI)
  4. Test data out (TDO)
  5. Test reset (TRST)

- Test bus uses both clock edges of the TCK:
  1) TMS and TDI are sampled on the rising edge of TCK
  2) TDO changes on the falling edge of TCK

TAP Signals

- **Test Clock (TCK):** The test clock input provides the clock for the test logic. TCK is a dedicated input that allows the serial test data path to be used independent of component-specific system clocks. It also permits shifting of test data concurrently with normal component operation.

- **Test Data Input (TDI):** TDI provides serial input for test instructions shifted into the Instruction Register and for data shifted through the Boundary Register or other data registers. Values are clocked into the selected register on a rising edge of TCK.

- **Test Data Output (TDO):** TDO is the serial output for test instructions and data from the Boundary Register or other data registers. The contents of the selected register (instruction or data) are shifted out on the falling edge of TCK.

TAP Signals (Cont..)

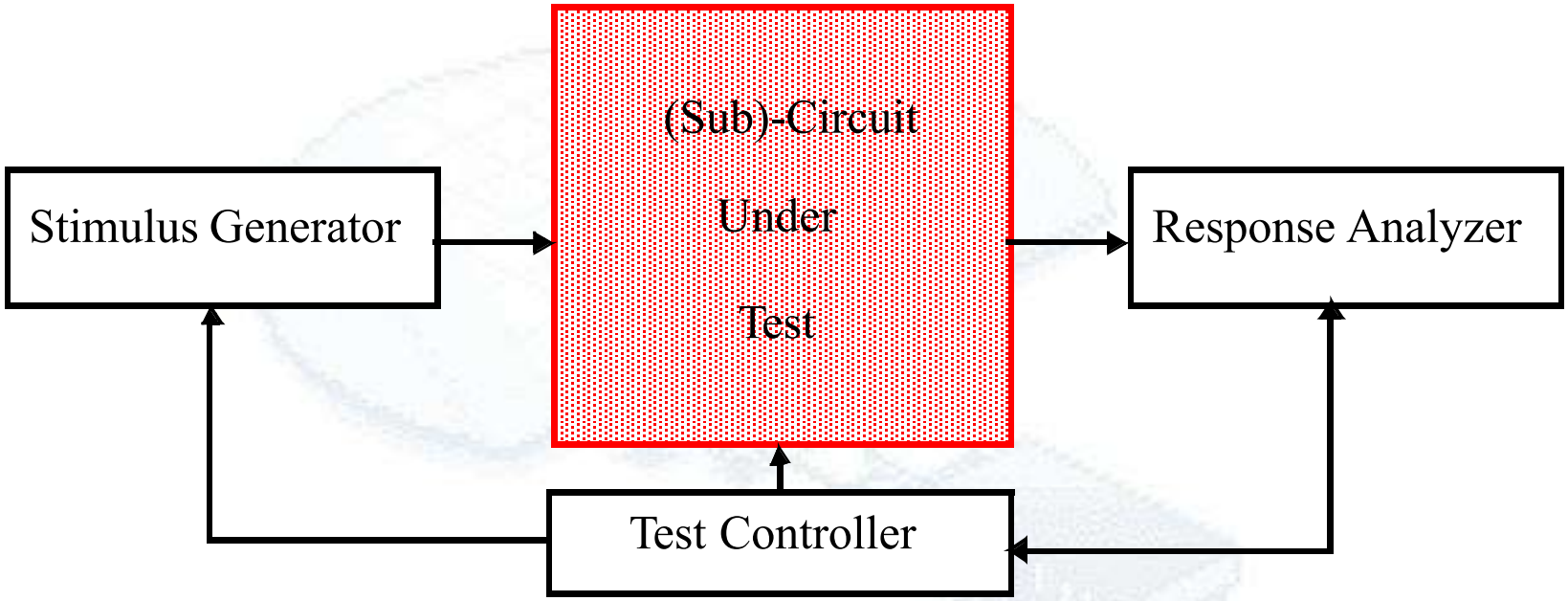
- **Test Mode Select (TMS):** The logic level of TMS, along with a rising edge applied to TCK, cause the movement from one state to another through the TAP controller. This, in turn, allows movement of data and TAP instructions through the state machine.

- **Test Reset (TRST*):** This optional input provides asynchronous initialization of the TAP Controller, which in turn causes asynchronous initialization of other test logic included in the design. The reset places the device in the normal operating mode and makes the Boundary Register inactive.

PROS and CONS of Boundary Scan

- Less overhead than Scan design
- Less expensive test equipment
- IC's tested at their complete, interconnected environment.
- Circuits with boundary scan are expensive and they can be hard to find
- Requires quite expensive software and equipment

Built-in Self-Test (BIST)



Rapidly becoming more important with increasing chip-complexity and larger modules

WHY BIST

- Since circuits today are more dense, faster, with smaller size, and that the logic-to-pin ratio on chips is increasing, it makes the testing of logic difficult.
- It takes longer time to generate test patterns and the patterns consume lot of memory.
- Therefore it has becoming important to implement different kind of logic into the design so it can test itself, which is what we called BIST.

PROS and CONS of BIST

- High fault coverage
- Able to run test at full speed
- All response analyzers have aliasing probability
- Requires quite much hardware to get good fault coverage.
- It is difficult to get a good BIST with less overhead to the circuit.

DFT Summary

- Main DFT techniques used today are Scan design, Built-in- Self-Test and Boundary scan.
- The choice of a DFT depends largely on its benefit-to-cost ratio.
- There are cost models used to help in this DFT decision, where factors like quality and volume are considered.

Self-Assess Questions

- A Full Scan Design replaces all normal flip-flops with Scan flip-flops. (True / False)
- Adding Scan design to a circuit will generally result in a decrease in pin count. (True / False)
- DFT logic improves the ability to observe and debug circuit performance (True / False)